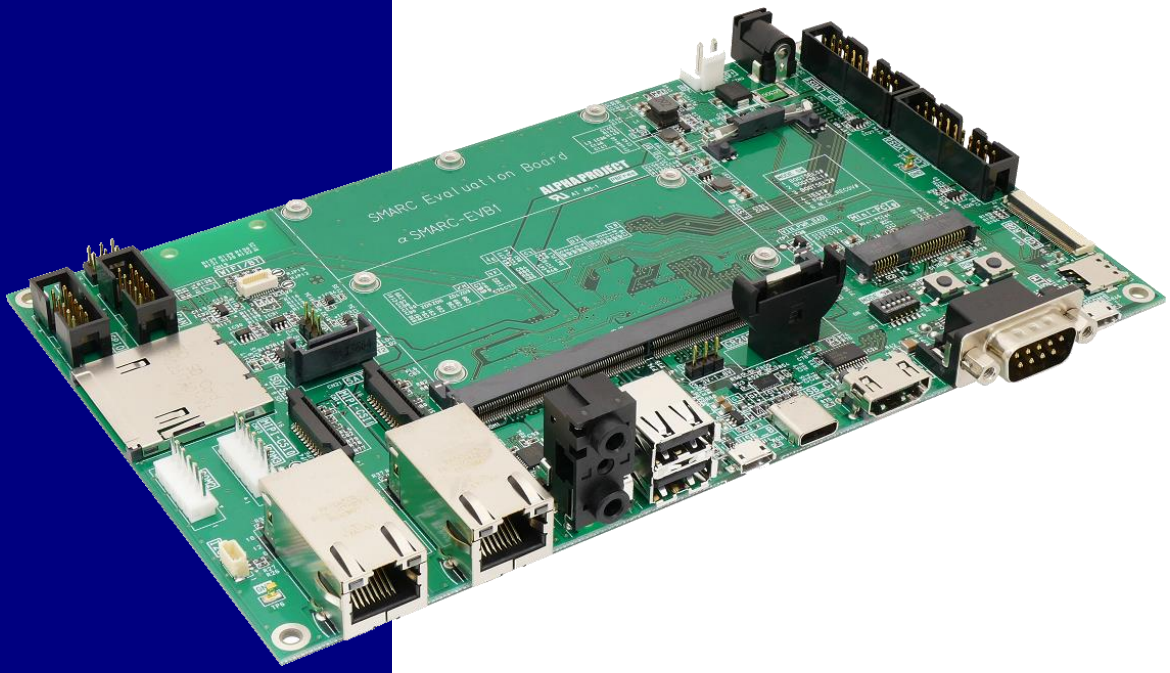
Alpha SoM Series

αSMARC-EVB1

SMARC Carrier Board

Hardware Manual

Rev 2.0



SMARC module

RoHS Compliant

ALPHA PROJECT

Important Information and Disclaimer

Thank you for purchasing an αSMARC-EVB1.
Please read this manual first in order to use this product correctly.
We appreciate your continued patronage of our products.

Product Includes

This module consists of the following components. Check the contents of the package, and if anything is missing, contact the vendor from which you purchased this product.

αSMARC-EVB1 Product Includes

●αSMARC-EVB1	x1	● Rubber feet	x4
● Manual / Warranty Info	x1		

■ Please understand that the contents and specifications of this module are subject to change without warning.

Handling Precautions

- ● General consumer electronic components are used in this product, and it was designed with the intent of using it for general consumer electronic equipment. Do not use this product in applications involving human life or accidents, or applications which may cause significant property damage, such as space, aviation, medical, nuclear power, transportation, traffic, and various safety devices.
- ● Do not use this product in environments with extremely hot or cold temperatures or strong vibrations.
- ● Do not use this product in water, or environments with high humidity or excessive oil.
- ● Do not use this product in environments with corrosive gas, flammable gas, etc.
- ● Do not turn on the power when the surface of the circuit board is wet or is contacting metal.
- ● Do not apply power that exceeds the rating.

■ Please understand that operation cannot be guaranteed in environments with excessive noise.
■ Beware that using the product in environments with continuous vibration (in vehicles, etc.) or impacts can shorten the product life or cause it to malfunction.
■ Turn off the power immediately if the product emits smoke, flame, or abnormal heat.
■ Beware that using this module in conditions that exceed the range of its specifications can cause it to malfunction.
■ Among the products and technologies listed in this manual, an export license based on the Foreign Exchange and Foreign Trade Law is required when exporting or taking out of Japan any items that fall under the regulated goods (technologies) stipulated in said law.
■ Alpha Project Co., Ltd. owns the copyright to the manual that comes with this product. It is prohibited to divert, post, transfer, or distribute this manual without permission.

Warranty

■ During the warranty period, if the product malfunctions during normal use while following precautions described in this manual, it will be covered by the warranty.
■ Regardless of whether or not the product is under warranty, Alpha Project Co., Ltd. will not compensate for any direct or indirect damage resulting from the operation of this product.
■ The warranty covers the main body of the product. The software, manuals, consumables, and packing boxes are not covered by the warranty.
■ This warranty is only valid in Japan. We do not accept requests from overseas.
■ For details on the product warranty regulations, see the attached warranty document or our website.

Reference Documents

Device and SMARC standard documents are published on the websites of various companies and organizations.
Consult them along with this manual.

■SMARC STANDARD (SGeT.ORG)

-SMARC Hardware Specification 2.1.1

- SMARC Design Guide Ver. 2.0

*About reference documents

- Documents and website URLs of various companies are subject to change without notice.
- Please direct inquiries about devices to the contact point of each device manufacturer.

Trademarks / License

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1. Overview

1.1 Product Overview

αSMARC-EVB1 is a carrier board that conforms to the SMARC2.1 standard.
Start application development for systems with SMARC modules immediately, reducing development time and costs.
It can be used for SMARC module evaluation, application development and prototyping purposes.

1.2 Functions and Features

■ Compliant with SMARC 2.1 standard

This product is compliant with the SMARC 2.1 standard, and can be operated immediately in combination with corresponding SoM.

■ Many interfaces

In addition to high-speed communication interfaces such as USB 3.0, PCI Express, Gigabit Ethernet, and SATA,
it has many peripheral functions such as LCD, AUDIO, MIPI-CSI2, and CAN.

■ Publication of circuit diagram

The circuit diagram of the carrier board has been publicized, so it can be used as a hardware reference.

The circuits of this product are just an example of design.
Please refer to the circuits of this product to design carrier boards for each user application.

1.3 Specifications Overview

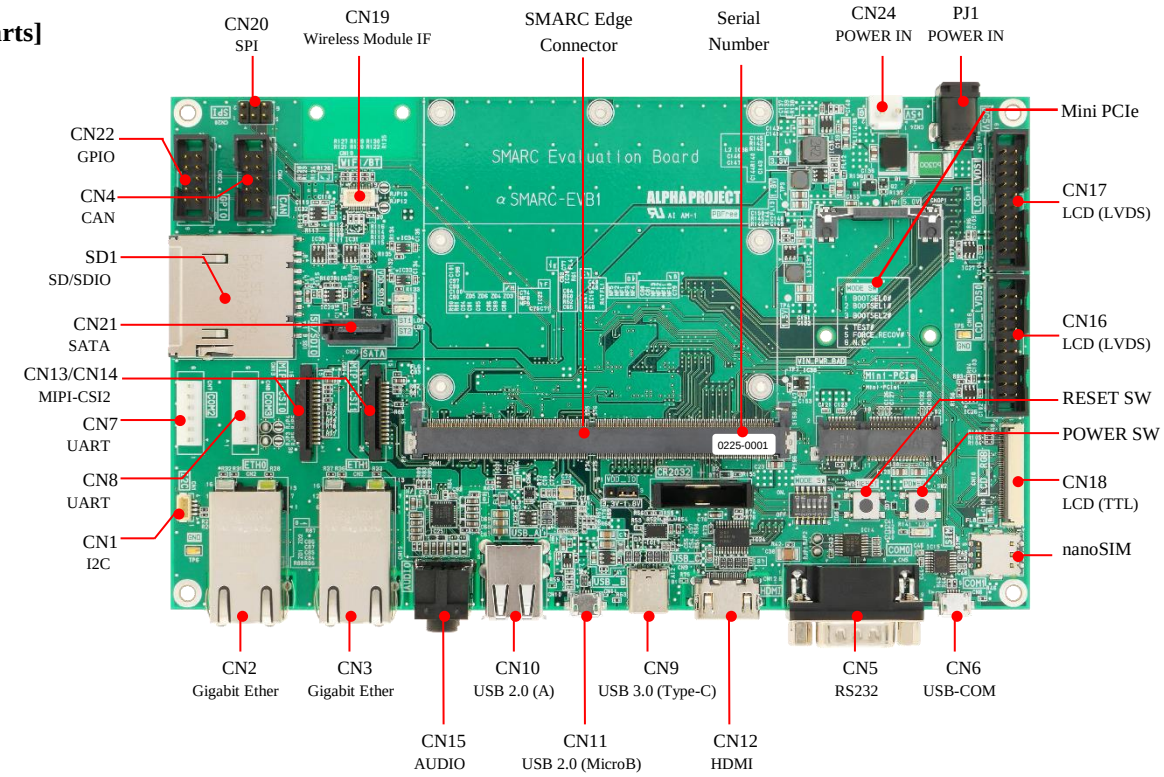
αSMARC-EVB1 Specifications

Function	Specifications
Compatible form factor	SMARC 2.1 Module Short/Full Size
Ethernet	Gigabit Ethernet × 2 ports
SD/SDIO	SD-CARD SLOT ×1
USB 2.0	USB-Host High Speed (Type-A) × 2 ports USB-Host High Speed (Type-A) / Function (Type-B Micro) × 1 port
USB 3.0	USB OTG SuperSpeed (Type-C) × 1 port
USB COM	USB/UART Bridge (Type-B Micro) × 1 port
PCI Express	mini PCIe SLOT ×1
SIM	nanoSIM SLOT ×1
LCD I/F (LVDS)	LVDS ×2
LCD I/F (TTL)	TTL (RGB666) ×1
HDMI	HDMI × 1 port
CAMERA	MIPI-CSI2 × 2 ports
SATA	SATA × 1 port
AUDIO	Stereo Line In/Out ×1
CAN	CAN × 2 ports (CAN-FD Support)
RS232	RS232 × 1 port
UART	TTL × 2 ports
Wireless Module Interface	Wireless Module “WM-RP-10” can be installed
I2C	I2C × 1 port (Grove IF)
LED	Monitor LED ×2 (GPIO) Power LED ×1
Backup Battery	CR2032 coin battery holder
Power Supply	DC 5.0 V ±5%
Current Consumption	Max. 1 W (EVB only, no external connection)
Use Environment Conditions	Temperature: -20 to +60˚ C (no condensation)
Dimensions	200 mm (W) × 120 mm (D)
Circuit Board	FR-4 (UL94-V0)
Environmental Support	RoHS directive (2015/863/EU)

Fig 1.3-1 Hardware Specifications

1.4 External Specifications

[Parts]



SMARC Module (Short Size) installed

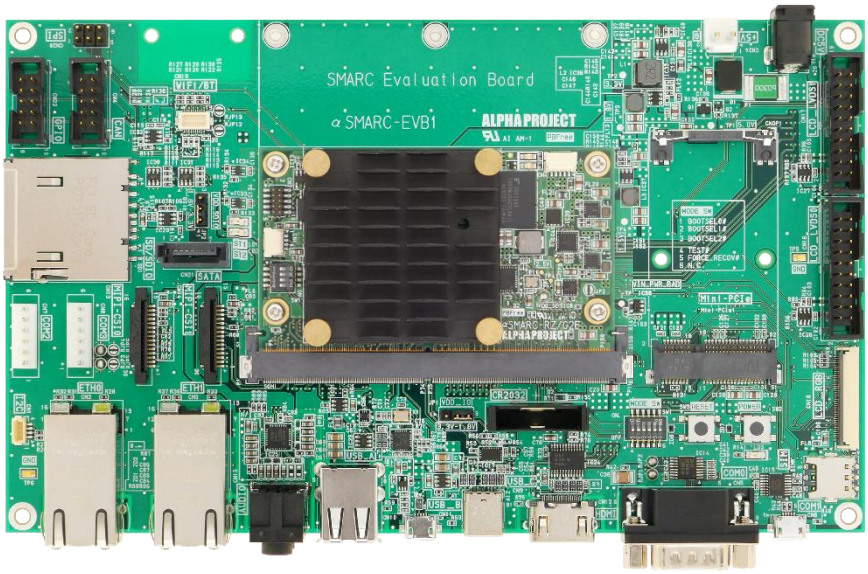


Fig 1.4-1 Board Overview

Part No.	Part Number/Manufacturer	Function	Remarks
CN1	BM04B-SRSS-TB /OMRON	I2C (Grove) Connector	
CN2	0826-1X1T-23-F /BelFuse	Gigabit Ether Connector (RJ-45)	
CN3	0826-1X1T-23-F /BelFuse	Gigabit Ether Connector (RJ-45)	
CN4	XG4C-1031 /OMRON	CAN IF Connector (MIL)	
CN5	XM2C-0942-132L /OMRON	RS232 IF Connector (D-SUB9)	
CN6	10104111-0001LF /FCI	USB COM Connector (Type-B Micro)	
CN7	B6P-SHF-1AA /JST	UART (TTL) IF Connector	
CN8	B6P-SHF-1AA /JST	UART (TTL) IF Connector	
CN9	124,015,980,000#2A /Amphenol	USB 3.0 Connector (Type-C)	
CN10	XM7A-0442-A /OMRON	USB 2.0 Connector (Type-A)	
CN11	10104111-0001LF /FCI	USB 2.0 Connector (Type-B Micro)	
CN12	10029449-111RLF /Amphenol	HDMI Connector	
CN13	1-1734248-5 /TE Connectivity	MIPI-CSI2 Connector	
CN14	1-1734248-5 /TE Connectivity	MIPI-CSI2 Connector	
CN15	STX-4235-3/3-N /KeyStone	AUDIO Jack (3.5 mm Mini)	
CN16	XG4C-2031 /OMRON	LCD (LVDS) IF Connector	
CN17	XG4C-2031 /OMRON	LCD (LVDS) IF Connector	
CN18	XF2M-4015-1A /OMRON	LCD (TTL) IF Connector	
CN19	DF12(3.0)-20DP-0.5V(86) /HIROSE	Wireless Module Interface Connector	
CN20	XG8T-0631 /OMRON	SPI Connector	
CN21	5607-5102-SH /3M	SATA Connector	
CN22	XG4C-1031 /OMRON	GPIO Connector	
CN24	B2P-VH /JST	Power IN	
PJ1	SM05B-SRSS-TB /JST	Power IN (AC-Adapter Jack)	
SD1	10067847-001RLF /Amphenol	SD/SDIO	
Mini-PCIe	MM60-52B1-B1-R850 /JAE	miniPCIe	
	MM60-EZH039-B5-R850 /JAE	miniPCIe (Latch)	
SIM	SIM8051-6-0-14-01-A /GCT	nanoSIM	
SoM	MM70-314B2-1-R500 /JAE	SMARC Edge Connector (MXM3.0)	

Table 1.4-2 Connector List

1.5 Circuit Configuration

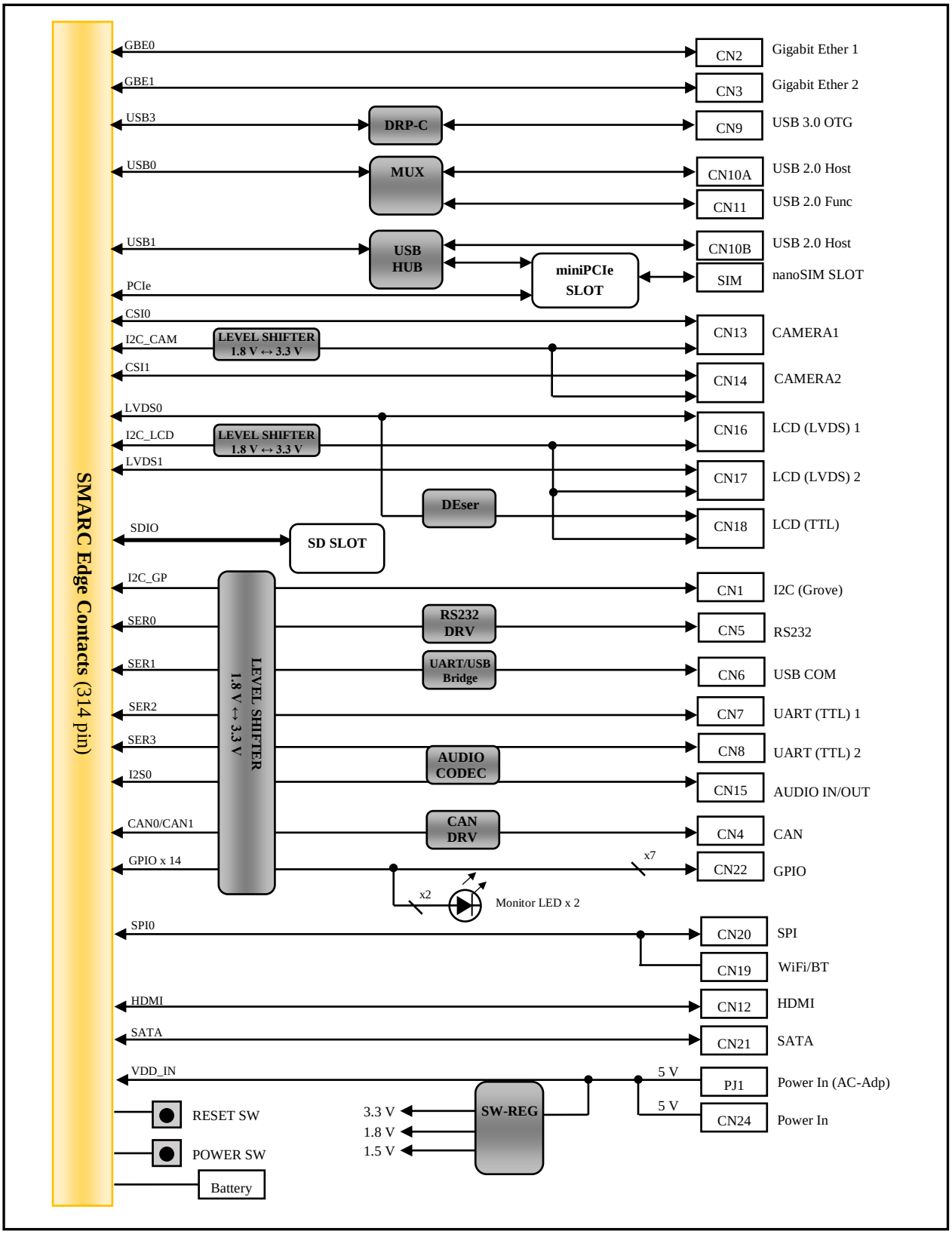


Fig 1.5-1 αSMARC-EVB Block Diagram

1.6 SMARC Interface Signals

SMARC interface signals supported by this product are listed below.

- Input/Output indicates the direction from the carrier board side.
- The signal name "*Signal name*" indicates that a signal is not yet used.
- "P.U" and "P.D" indicate pull-up or pull-down within SoM.
- "x" in voltage indicates it conforms to the standard of each interface.
- "SW" in voltage indicates it is connected to a Switch (contact).
- VDD_IO can be set to 1.8 V (standard) or 3.3 V. For details, see "1.9.1 VDD_IO Settings".

For definitions of each signal in the SMARC standard, see the SMARC standard specification.

SMARC Hardware Specification 2.1.1 **https://www.sget.org/standards/smarc/**

Table 1.6-1 SMARC interface signal assignment

No.	Signal Name	Input/ Output	Voltage	Remarks	No.	Signal Name	Input/ Output	Voltage	Remarks
P1	*SMB_ALERT#*				S1	I2C_CAM1_CK	In	VDD_IO	
P2	GND		GND		S2	I2C_CAM1_DAT	I/O	VDD_IO	
P3	CSI1_CK+	Out	x		S3	GND		GND	
P4	CSI1_CK-	Out	x		S4	*RSVD*			
P5	*GBE1_SDP*				S5	I2C_CAM0_CK	In	VDD_IO	
P6	*GBE0_SDP*				S6	*CAM_MCK*			
P7	CSI1_RX0+	out	x		S7	I2C_CAM0_DAT	I/O	VDD_IO	
P8	CSI1_RX0-	out	x		S8	CSI0_CK+	Out	x	
P9	GND		GND		S9	CSI0_CK-	Out	x	
P10	CSI1_RX1+	Out	x		S10	GND		GND	
P11	CSI1_RX1-	Out	x		S11	CSI0_RX0+	In	x	
P12	GND	In	GND		S12	CSI0_RX0-	In	x	
P13	*CSI1_RX2+*				S13	GND		GND	
P14	*CSI1_RX2-*				S14	CSI0_RX1+	Out	x	
P15	GND		GND		S15	CSI0_RX1-	Out	x	
P16	*CSI1_RX3+*				S16	GND		GND	
P17	*CSI1_RX3-*				S17	GBE1_MDI0+	I/O	x	
P18	GND		GND		S18	GBE1_MDI0-	I/O	x	
P19	GBE0_MDI3-	I/O	x		S19	GBE1_LINK100#	In	3.3 V	
P20	GBE0_MDI3+	I/O	x		S20	GBE1_MDI1+	I/O	x	
P21	GBE0_LINK100#	In	3.3 V		S21	GBE1_MDI1-	I/O	x	
P22	GBE0_LINK1000#	In	3.3 V		S22	GBE1_LINK1000#	In	3.3 V	
P23	GBE0_MDI2-	I/O	x		S23	GBE1_MDI2+	I/O	x	
P24	GBE0_MDI2+	I/O	x		S24	GBE1_MDI2-	I/O	x	
P25	GBE0_LINK_ACT#	In	3.3 V		S25	GND		GND	
P26	GBE0_MDI1-	I/O	x		S26	GBE1_MDI3+	I/O	x	
P27	GBE0_MDI1+	I/O	x		S27	GBE1_MDI3-	I/O	x	
P28	*GBE0_CTREF*	Out	x		S28	*GBE1_CTREF*		x	

P29	GBE0_MDI0-	I/O	x	
P30	GBE0_MDI0+	I/O	x	
P31	*SPIO_CS1#*			
P32	GND		GND	
P33	SDIO_WP	Out	3.3 V	
P34	SDIO_CMD	I/O	3.3 V/1.8 V	
P35	SDIO_CD#	Out	3.3 V	
P36	SDIO_CK	In	3.3 V/1.8 V	
P37	SDIO_PWR_EN	In	3.3 V	
P38	GND		GND	
P39	SDIO_D0	I/O	3.3 V/1.8 V	
P40	SDIO_D1	I/O	3.3 V/1.8 V	
P41	SDIO_D2	I/O	3.3 V/1.8 V	
P42	SDIO_D3	I/O	3.3 V/1.8 V	
P43	SPI0_CS0#	In	VDD_IO	
P44	SPI0_CK	In	VDD_IO	
P45	SPI0_DIN	Out	VDD_IO	
P46	SPI0_DO	In	VDD_IO	
P47	GND		GND	
P48	SATA_TX+	In	x	
P49	SATA_TX-	In	x	
P50	GND		GND	
P51	SATA_RX+	Out	x	
P52	SATA_RX-	Out	x	
P53	GND		GND	
P54	*ESPI_CS0#*			
P55	*ESPI_CS1#*			
P56	*ESPI_CK#*			
P57	*ESPI_IO_1#*			
P58	*ESPI_IO_0#*			
P59	GND		GND	
P60	USB0+	I/O	x	
P61	USB0-	I/O	x	
P62	USB0_EN_OC#	I/O	3.3 V O.D	
P63	USB0_VBUS_DET	Out	5 V	
P64	*USB0_OTG_ID*			
P65	USB1+	I/O	x	
P66	USB1-	I/O	x	
P67	USB1_EN_OC#	I/O	3.3 V O.D	
P68	GND		GND	
P69	*USB2+*			
P70	*USB2-*			
P71	*USB2_EN_OC#*			
P72	*RSVD*			
P73	*RSVD*			
P74	USB3_EN_OC#	I/O	3.3V O.D	

S29	PCIE_D_TX+	In	x	
S30	PCIE_D_TX-	In	x	
S31	GBE1_LINK_ACT#	In	3.3 V	
S32	*PCIE_D_RX+*	Out	x	
S33	*PCIE_D_RX-*	Out	x	
S34	GND		GND	
S35	*USB4+*	I/O	x	
S36	*USB4-*	I/O	x	
S37	USB3_VBUS_DET	Out	5 V	
S38	AUDIO_MCK	In	VDD_IO	
S39	I2S0_LRCK	I/O	VDD_IO	
S40	I2S0_SDOUT	In	VDD_IO	
S41	I2S0_SDIN	Out	VDD_IO	
S42	I2S0_CK	I/O	VDD_IO	
S43	*ESPI_ALERT0#*			
S44	*ESPI_ALERT1#*			
S45	*MDIO_CLK*			
S46	*MDIO_DAT*			
S47	GND		GND	
S48	I2C_GP_CK	In	VDD_IO	
S49	I2C_GP_DAT	I/O	VDD_IO	
S50	*HDA_SYNC*			
S51	*HDA_SDO*			
S52	*HDA_SDI*			
S53	*HDA_CK*			
S54	*SATA_ACT#*			
S55	*USB5_EN_OC#*			
S56	*ESPI_IO_2*			
S57	*ESPI_IO_3*			
S58	*ESPI_RESET#*			
S59	*USB5+*			
S60	*USB5-*			
S61	GND		GND	
S62	USB3_SSTX+	In	x	
S63	USB3_SSTX-	In	x	
S64	GND		GND	
S65	USB3_SSRX+	Out	x	
S66	USB3_SSRX-	Out	x	
S67	GND		GND	
S68	USB3+	I/O	x	
S69	USB3-	I/O	x	
S70	GND		GND	
S71	*USB2_SSTX+*			
S72	*USB2_SSTX-*			
S73	GND		GND	
S74	*USB2_SSRX+*			

P75	PCIE_A_RST#	In	3.3 V	
P76	*USB4_EN_OC#*	I/O	3.3 V	
P77	*PCIE_B_CKREQ*			
P78	*PCIE_A_CKREQ*			
P79	GND		GND	
P80	*PCIE_C_REFCK+*			
P81	*PCIE_C_REFCK-*			
P82	GND		GND	
P83	PCIE_A_REFCK+	In	x	
P84	PCIE_A_REFCK-	In	x	
P85	GND		GND	
P86	PCIE_A_RX+	Out	x	
P87	PCIE_A_RX-	Out	x	
P88	GND		GND	
P89	PCIE_A_TX+	In	x	
P90	PCIE_A_TX-	In	x	
P91	GND		GND	
P92	HDMI_D2+	In	x	
P93	HDMI_D2-	In	x	
P94	GND		GND	
P95	HDMI_D1+	In	x	
P96	HDMI_D1-	In	x	
P97	GND		GND	
P98	HDMI_D0+	In	x	
P99	HDMI_D0-	In	x	
P100	GND		GND	
P101	HDMI_CK+	In	x	
P102	HDMI_CK-	In	x	
P103	GND		GND	
P104	HDMI_HPD	Out	1.8 V	
P105	HDMI_CTRL_CK	In	1.8 V	
P106	HDMI_CTRL_DAT	I/O	1.8 V	
P107	*DP1_AUX_SEL*			
P108	GPIO0	I/O	VDD_IO	
P109	GPIO1	I/O	VDD_IO	
P110	GPIO2	I/O	VDD_IO	
P111	GPIO3	I/O	VDD_IO	
P112	GPIO4	I/O	VDD_IO	
P113	GPIO5	I/O	VDD_IO	
P114	GPIO6	I/O	VDD_IO	
P115	GPIO7	I/O	VDD_IO	
P116	GPIO8	I/O	VDD_IO	
P117	GPIO9	I/O	VDD_IO	
P118	GPIO10	I/O	VDD_IO	
P119	GPIO11	I/O	VDD_IO	
P120	GND		GND	

S75	*USB2_SSRX-*			
S76	*PCIE_B_RST#*			
S77	*PCIE_C_RST#*			
S78	*PCIE_C_RX+*			
S79	*PCIE_C_RX-*			
S80	GND		GND	
S81	*PCIE_C_TX+*			
S82	*PCIE_C_TX+*			
S83	GND		GND	
S84	*PCIE_B_REFCK+*			
S85	*PCIE_B_REFCK+*			
S86	GND		GND	
S87	*PCIE_B_RX+*			
S88	*PCIE_B_RX-*			
S89	GND		GND	
S90	*PCIE_B_TX+*			
S91	*PCIE_B_TX-*			
S92	GND		GND	
S93	*DP0_LANE0+*			
S94	*DP0_LANE0-*			
S95	*DP0_AUX_SEL*			
S96	*DP0_LANE1+*			
S97	*DP0_LANE1-*			
S98	*DP0_HPD*			
S99	*DP0_LANE2+*			
S100	*DP0_LANE2-*			
S101	GND		GND	
S102	*DP0_LANE3+*			
S103	*DP0_LANE3-*			
S104	USB3_OTG_ID	Out	3.3 V	
S105	*DP0_AUX+*			
S106	*DP0_AUX-*			
S107	LCD1_BKLT_EN	In	VDD_IO	
S108	LVDS1_CK+	In	x	
S109	LVDS1_CK-	In	x	
S110	GND		GND	
S111	LVDS1_0+	In	x	
S112	LVDS1_0-	In	x	
S113	*ePD1_HPD*			
S114	LVDS1_1+	In	x	
S115	LVDS1_1-	In	x	
S116	LCD1_VDD_EN	In	VDD_IO	
S117	LVDS1_2+	In	x	
S118	LVDS1_2-	In	x	
S119	GND		GND	
S120	LVDS1_3+	In	x	

P121	I2C_PM_CK	I/O	VDD_IO	
P122	I2C_PM_DAT	I/O	VDD_IO	
P123	BOOT_SEL0#	Out	SW	
P124	BOOT_SEL1#	Out	SW	
P125	BOOT_SEL2#	Out	SW	
P126	RESET_OUT#	In	VDD_IO	
P127	RESET_IN#	Out	SW	
P128	POWER_BTN#	Out	SW	
P129	SER0_TX	In	VDD_IO	
P130	SER0_RX	Out	VDD_IO	
P131	SER0_RTS#	In	VDD_IO	
P132	SER0_CTS#	Out	VDD_IO	
P133	GND		GND	
P134	SER1_TX	In	VDD_IO	
P135	SER1_RX	Out	VDD_IO	
P136	SER2_TX	In	VDD_IO	
P137	SER2_RX	Out	VDD_IO	
P138	SER2_RTS#	In	VDD_IO	
P139	SER2_CTS#	Out	VDD_IO	
P140	SER3_TX	In	VDD_IO	
P141	SER3_RX	Out	VDD_IO	
P142	GND		GND	
P143	CAN0_TX	In	VDD_IO	
P144	CAN0_RX	Out	VDD_IO	
P145	CAN1_TX	In	VDD_IO	
P146	CAN1_RX	Out	VDD_IO	
P147	VDD_IN	Out	4.75 - 5.25 V	
P148	VDD_IN	Out	4.75 - 5.25 V	
P149	VDD_IN	Out	4.75 - 5.25 V	
P150	VDD_IN	Out	4.75 - 5.25 V	
P151	VDD_IN	Out	4.75 - 5.25 V	
P152	VDD_IN	Out	4.75 - 5.25 V	
P153	VDD_IN	Out	4.75 - 5.25 V	
P154	VDD_IN	Out	4.75 - 5.25 V	
P155	VDD_IN	Out	4.75 - 5.25 V	
P156	VDD_IN	Out	4.75 - 5.25 V	

S121	LVDS1_3-	In	x	
S122	LCD1_BKLT_PWM	In	VDD_IO	
S123	GPIO13	I/O	VDD_IO	
S124	GND		GND	
S125	LVDS0_0+	In	x	
S126	LVDS0_0-	In	x	
S127	LCD0_BKLT_EN	In	VDD_IO	
S128	LVDS0_1+	In	x	
S129	LVDS0_1-	In	x	
S130	GND		GND	
S131	LVDS0_2+	In	x	
S132	LVDS0_2-	In	x	
S133	LCD0_VDD_EN	In	VDD_IO	
S134	LVDS0_CK+	In	x	
S135	LVDS0_CK-	In	x	
S136	GND		GND	
S137	LVDS0_3+	In	x	
S138	LVDS0_3-	In	x	
S139	I2C_LCD_CK	In	VDD_IO	
S140	I2C_LCD_DAT	I/O	VDD_IO	
S141	LCD0_BKLT_PWM	In	VDD_IO	
S142	GPIO12	I/O	VDD_IO	
S143	GND		GND	
S144	*ePD0_HPD*			
S145	WDT_TIME_OUT#	In	VDD_IO	
S146	PCIE_WAKE#	Out	3.3 V	
S147	VDD_RTC	Out	2.0 V - 3.25 V	
S148	*LID#*			
S149	*SLEEP#*			
S150	VIN_PWR_BAD#	Out	VDD_IN	
S151	*CHARGING#*			
S152	*CHARGER_PRSNT#*			
S153	CARRIER_STBY#	In	VDD_IO	
S154	CARRIER_PWR_ON	In	VDD_IO	
S155	FORCE_RECOV#	Out	SW	
S156	*BATLOW#*			
S157	TEST#	Out	SW	
S158	GND		GND	

1.7 Supported SoM

The SMARC SoM and functions supported by this product are as follows.

[αSMARC_RZ/G2E]

Part No.	Carrier Board Function	SoM supported function	Remarks
CN1	I2C (Grove) Connector	I2C_GP	
CN2	Gigabit Ether Connector (RJ-45)	GBE0 (100/1000 BASE)	
CN3	Gigabit Ether Connector (RJ-45)	*Not Supported*	
CN4	CAN IF Connector (MIL)	CAN0, CAN1	
CN5	RS232 IF Connector (D-SUB9)	SER0	
CN6	USB COM Connector (Type-B Micro)	SER1	
CN7	UART (TTL) IF Connector	SER2	
CN8	UART (TTL) IF Connector	*Not Supported*	
CN9	USB 3.0 Connector (Type-C)	USB3SS, USB3	
CN10	USB2.0 Connector (Type-A upper)	*Not Supported*	
CN10	USB2.0 Connector (Type-A Lower)	USB1 (Host)	
CN11	USB 2.0 Connector (Type-B Micro)	USB0 (Function)	
CN12	HDMI Connector	*Not Supported*	
CN13	MIPI-CSI2 Connector	*Not Supported*	
CN14	MIPI-CSI2 Connector	CSI1	
CN15	AUDIO Jack (3.5 mm Mini)	I2S0	
CN16	LCD (LVDS) IF Connector	LVDS0	
CN17	LCD (LVDS) IF Connector	LVDS1	
CN18	LCD (TTL) IF Connector	LVDS0	
CN19	Wireless Module Interface Connector	SPI0	
CN20	SPI Connector	SPI0	
CN21	SATA Connector	*Not Supported*	
CN22	GPIO Connector	GPIO [0,1,3,4,11,12,13]	
SD1	SD/SDIO	SD0	
Mini-PCIe	miniPCIe	PCIe_A	
LD1, LD2	ST1, ST2	GPIO [12,13]	
SW1	MODE SW	BOOT_SEL#[0,2],TEST#,FORCE_RECV#	
SW2	Power Button	POWER_BTN#	
SW3	Reset Button	RESET_IN#	
BT1	Battery Holder	VDD_RTC	

Table 1.7-1 αSMARC-RZ/G2E function support

[αSMARC_IMX8MM]

Part No.	Carrier Board Function	SoM supported function	Remarks
CN1	I2C(Grove) Connector	I2C_GP	
CN2	Gigabit Ether Connector (RJ-45)	GBE0(100/1000BASE)	
CN3	Gigabit Ether Connector (RJ-45)	*Not Support*	
CN4	CAN IF Connector (MIL)	CAN0 (CAN1 *Not Support*)	
CN5	RS232 IF Connector (D-SUB9)	SER0	
CN6	USB COM Connector (Type-B Micro)	SER1	
CN7	UART(TTL) IF Connector	SER2	
CN8	UART(TTL) IF Connector	*Not Support*	
CN9	USB3.0 Connector (Type-C)	*Not Support*	
CN10	USB2.0 Connector (Type-A upper)	USB0(Host)	Exclusive
CN10	USB2.0 Connector (Type-A Lower)	USB1(Host)	
CN11	USB2.0 Connector (Type-B Micro)	USB0(Function)	Exclusive
CN12	HDMI Connector	*Not Support*	
CN13	MIPI-CSI2 Connector	*Not Support*	
CN14	MIPI-CSI2 Connector	CSI1	
CN15	AUDIO Jack (3.5mm Mini)	I2S0	
CN16	LCD(LVDS) IF Connector	LVDS0	
CN17	LCD(LVDS) IF Connector	LVDS1	
CN18	LCD(TTL) IF Connector	LVDS0	
CN19	Wireless Module Interface Connector	SPI0	
CN20	SPI Connector	SPI0	
CN21	SATA Connector	*Not Support*	
CN22	GPIO Connector	GPIO[0,1,3,4,11,12,13]	
SD1	SD/SDIO	SD2	
Mini-PCIe	miniPCIe	PCIe_A	
LD1,LD2	ST1,ST2	GPIO[12,13]	
SW1	MODE SW	BOOT_SEL#[0,1,2],TEST#,FORCE_RECV#	
SW2	Power Button	POWER_BTN#	
SW3	Reset Button	RESET_IN#	
BT1	Battery Holder	VDD_RTC	

* “LCD-KIT-D02” in section 4.5 is not supported with αSMARC-IMX8MM by not compatible on output signal frequency of SoM.

Table 1.7-2 αSMARC-IMX8MM function support

[αSMARC_IMX8MN]

Part No.	Carrier Board Function	SoM supported function	Remarks
CN1	I2C(Grove) Connector	I2C_GP	
CN2	Gigabit Ether Connector (RJ-45)	GBE0(100/1000BASE)	
CN3	Gigabit Ether Connector (RJ-45)	*Not Support*	
CN4	CAN IF Connector (MIL)	CAN0 (CAN1 *Not Support*)	
CN5	RS232 IF Connector (D-SUB9)	SER0	
CN6	USB COM Connector (Type-B Micro)	SER1	
CN7	UART(TTL) IF Connector	SER2	
CN8	UART(TTL) IF Connector	*Not Support*	
CN9	USB3.0 Connector (Type-C)	*Not Support*	
CN10	USB2.0 Connector (Type-A upper)	USB0(Host)	Exclusive
CN10	USB2.0 Connector (Type-A Lower)	USB0(Host)	Exclusive
CN11	USB2.0 Connector (Type-B Micro)	USB0(Function)	Exclusive
CN12	HDMI Connector	*Not Support*	
CN13	MIPI-CSI2 Connector	*Not Support*	
CN14	MIPI-CSI2 Connector	CSI1	
CN15	AUDIO Jack (3.5mm Mini)	I2S0	
CN16	LCD(LVDS) IF Connector	LVDS0	
CN17	LCD(LVDS) IF Connector	LVDS1	
CN18	LCD(TTL) IF Connector	LVDS0	
CN19	Wireless Module Interface Connector	SPI0	
CN20	SPI Connector	SPI0	
CN21	SATA Connector	*Not Support*	
CN22	GPIO Connector	GPIO[0,1,3,4,11,12,13]	
SD1	SD/SDIO	SD0	
Mini-PCIe	miniPCIe	*Not Support*	
LD1,LD2	ST1,ST2	GPIO[12,13]	
SW1	MODE SW	BOOT_SEL#[0,1,2],TEST#,FORCE_RECV#	
SW2	Power Button	POWER_BTN#	
SW3	Reset Button	RESET_IN#	
BT1	Battery Holder	VDD_RTC	

* “LCD-KIT-D02” in section 4.5 is not supported with αSMARC-IMX8MN by not compatible on output signal frequency of SoM.

Table 1.7-3 αSMARC-IMX8MN function support

1.8 Installing SMARC SoM

Install a SMARC module by plugging it into a card-edge connector on the carrier board.

The card edge connector is fragile, so handle it with adequate care.

Also, be careful not to allow dust or foreign objects to get caught in the contact area of the card-edge.

[Installation Method]

1. Insert the SMARC module diagonally (at an angle of about 30°) into the card-edge connector of the carrier board.
2. With the SMARC module inserted into the card-edge connector, push it down so that it is parallel to the carrier board.
3. Secure the SMARC module with screws.

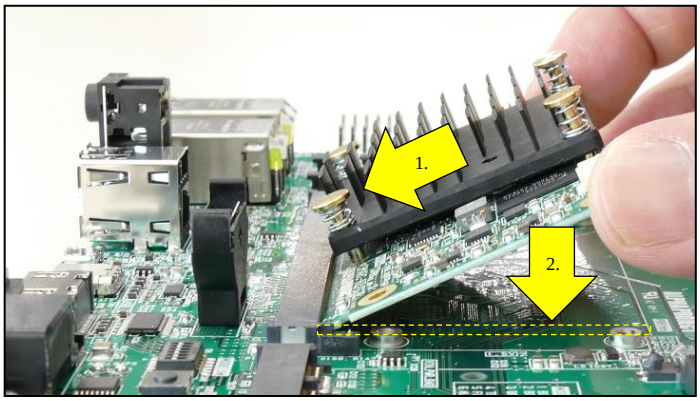


Fig 1.8-1 Installation to carrier board

1.9 Settings

Check that jumper settings are correct before turning on the power.

There are VDD_IO(JP1) and VDD_SDIO(JP2) settings. Normally, there is no problem with keeping the factory settings.

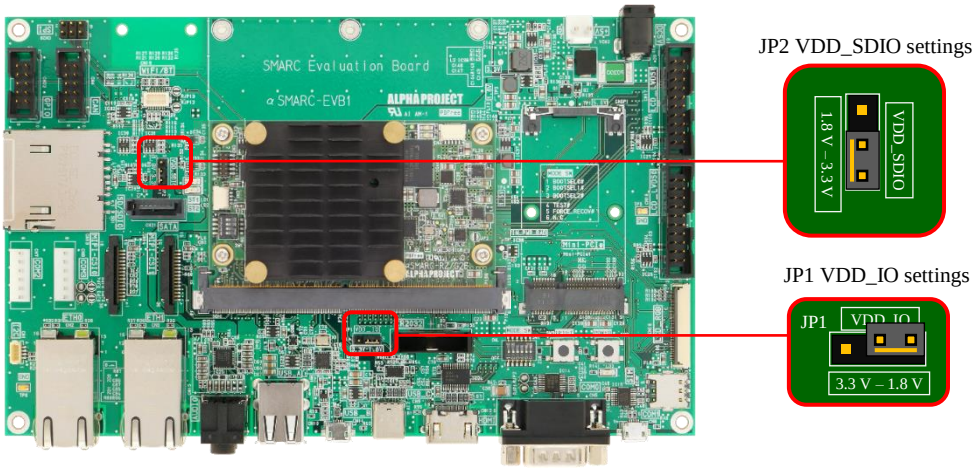


Fig 1.9-1 JP settings

1.9.1 VDD_IO Settings

The I/O voltage of the SMARC interface is basically defined as 1.8 V,

but some αSMARC SoM products support an I/O voltage of 3.3V. To support these products, the I/O voltage of the SMARC interface can be switched to 3.3 V.

Note that the 3.3V setting is not normal with the SMARC standard.

JP1	Remarks
1.8 V(SMARC standard)	Factory settings
3.3 V	
Make sure to match the voltage setting with the SoM setting. Damage can result from not doing this. Also, set JP1 to 1.8 V or 3.3 V and do not leave it open.	

Table 1.9.2 VDD_IO settings

1.9.2 VDD_SDIO Settings

It is possible to select 3.3 V or 1.8 V for the power supply of the SD card.

Currently, there is basically no problem with the 3.3 V setting.

(The UHS-I 1.8 V signal is supported by the interface function on the SoM side.)

JP2	Remarks
3.3 V(SMARC standard)	Factory settings
1.8 V	
Be sure to set JP2 and do not leave it open.	

Table 1.9-3 VDD_SDIO settings

1.10 Startup Check

αSMARC-EVB1 is preloaded with a Linux image when shipped.

The following is a description of how to do a startup check of αSMARC-EVB1.

SMARC SoM: αSMARC-RZ/G2E

1. Connect a PC and power supply

   Attach SMARC SoM to αSMARC-EVB1 and connect the PC and AC adapter (power supply) as follows.

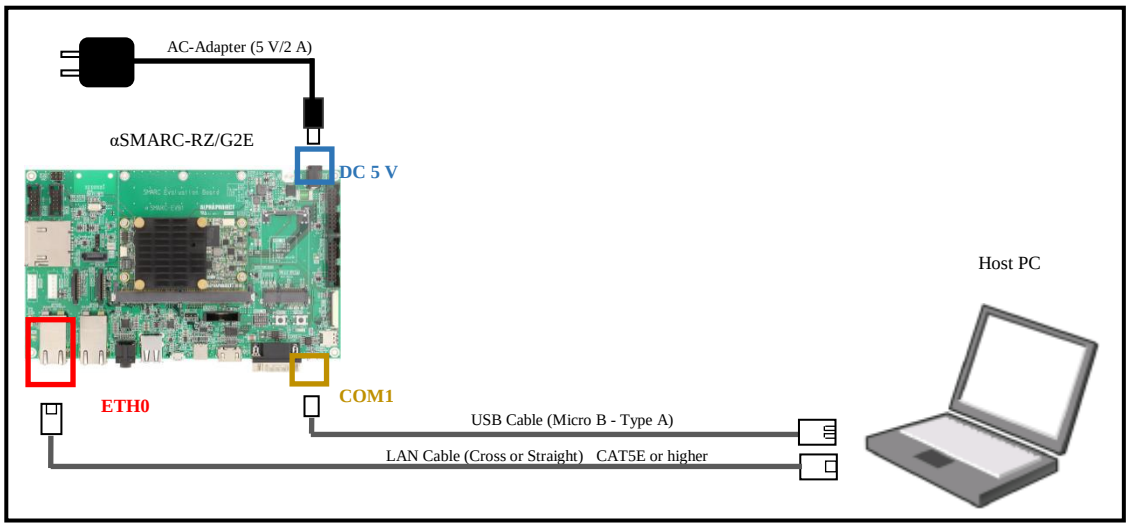


Fig 1.10-1 Connection for startup check

2. Check the settings

   Before turning on the power, check that the switches of αSMARC-RZ/G2E and αSMARC-EVB1 are set as follows.

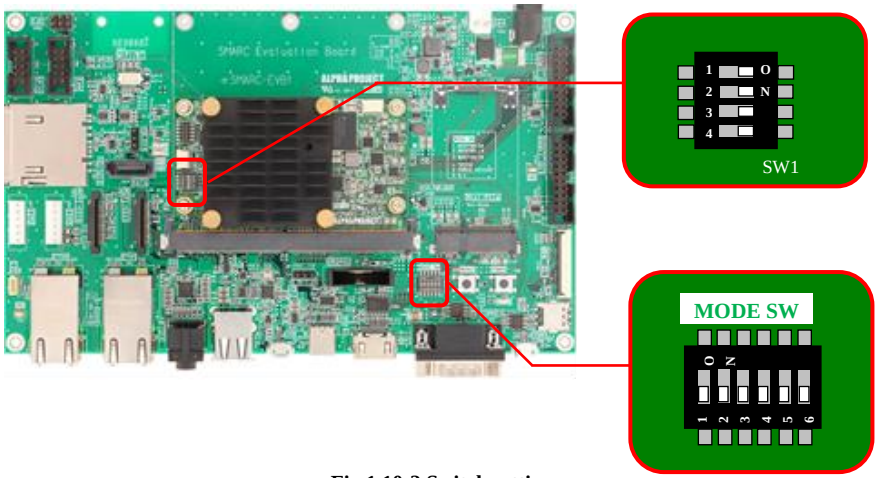


Fig 1.10-2 Switch settings

3. COM port number check

Press the POWER switch to turn on the power.

The virtual COM port is recognized on the host PC, so check the COM port number.

On Windows, “USB Serial Port (COMxx)” is displayed under “Ports (COM and LPT)” in “Device Manager”. (xx is a number)

4. Preparation and setting of terminal software

Install terminal software such as Tera Term on the host OS (Windows) and set communication values as follows.

Setting Item	Setting Value
Port Number	Virtual COM port
Communication Speed	115200 bps
Data Length	8 bit
Stop Bit	1 bit
Parity	None
Flow Control	None

Table 1.10-3 Connection setting

5. Turn the power ON

When the POWER switch is pressed, the power turns on, the Power LED lights up, the Linux kernel automatically starts, and the startup log is displayed on the terminal software of the PC. It takes about 10 to 20 seconds for everything to start up.

```
NOTICE:  BL2: DRAM Split is OFF
NOTICE:  BL2: QoS is default setting (rev.0.05)
NOTICE:  BL2: DRAM refresh interval 3.9 usec
NOTICE:  BL2: CH0: 400,000,000 - 43ffffff, 1 GiB
NOTICE:  BL2: FDT at 0xe6312438

        :
    <Partially omitted>
        :

Poky (Yocto Project Reference Distro) 2.4.3 asmarc-rzg2e ttySC0

BSP: RZG2E/aSMARC-RZG2E/1.0.6
LSI: RZG2E
Version: 1.0.6
asmarc-rzg2e login:
```

* The message may differ depending on the version and environment.

Fig 1.10-4 Startup Log (Terminal)

6. Turn the power OFF

When the POWER switch is pressed again, shutdown processing is done and the power is automatically turned off. (Power LED off)

It takes about 5 seconds to turn off the power.

2. Functions

2.1 LCD (LVDS)

LCD (LVDS) supports two channels, LVDS0 and LVDS1.

The connector connects to LCD0 (CN16) and LCD1 (CN17) with a 2.5 mm x 2 row box pin header.

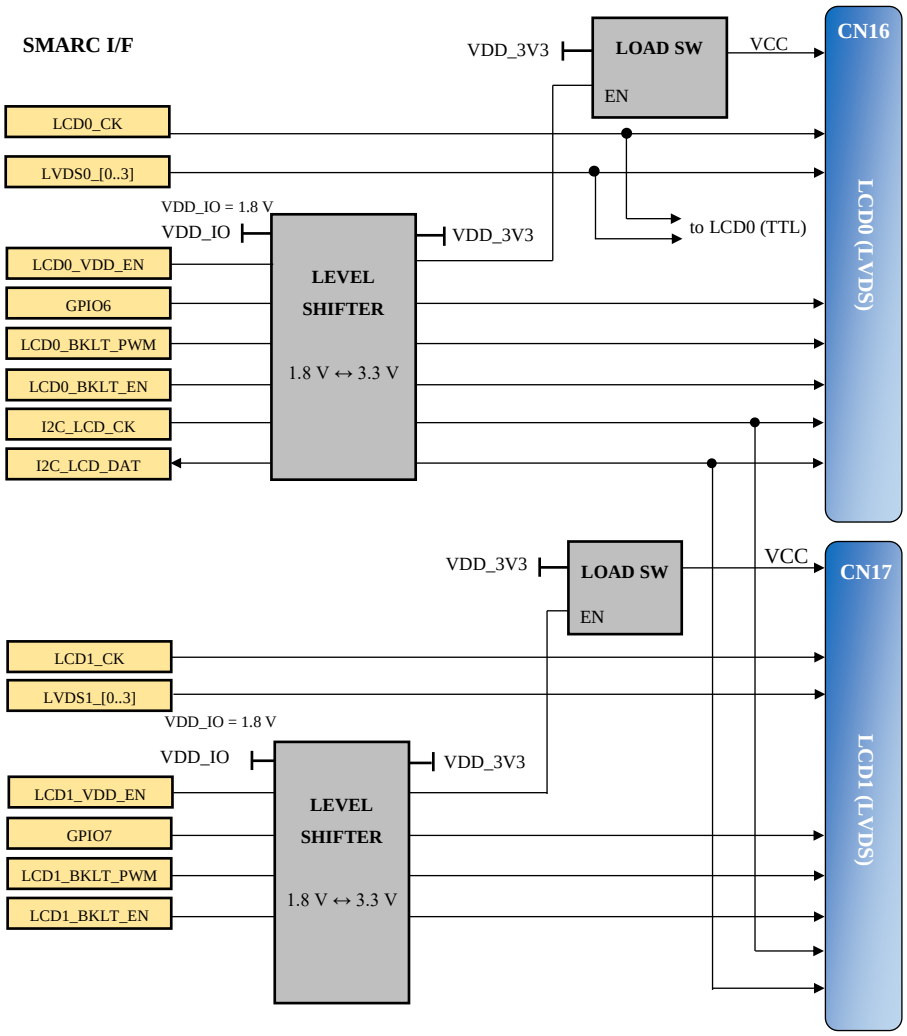


Fig 2.1-1 LCD (LVDS) circuit connection configuration

LCD0 [CN16]

No	Signal Name	Description	SMARC Signal Path	Remarks
1	VCC	+3.3 V		
2	VCC	+3.3 V		
3	GND	GND		
4	GND	GND		
5	LVDS0-	LCD DATA	LVDS0_0-	
6	LVDS0+	LCD DATA	LVDS0_0+	
7	LVDS1-	LCD DATA	LVDS0_1-	
8	LVDS1+	LCD DATA	LVDS0_1+	
9	LVDS2-	LCD DATA	LVDS0_2-	
10	LVDS2+	LCD DATA	LVDS0_2+	
11	LVDS3-	LCD DATA	LVDS0_3-	
12	LVDS3+	LCD DATA	LVDS0_3+	
13	LVDS_CLK-	LCD DATA	LVDS0_CK-	
14	LVDS_CLK+	LCD DATA	LVDS0_CK+	
15	GND	GND		
16	UD/GPIO	UD Control/GPIO	GPIO6	3.3 V
17	BKLT_PWM	BackLight PWM	LCD0_BKLT_PWM	3.3 V
18	BKLT_EN	BackLight ENABLE	LCD0_BKLT_EN	3.3 V
19	I2C_CK	I2C CLOCK	I2C_LCD_CK	3.3 V
20	I2C_DAT	I2C DATA	I2C_LCD_DAT	3.3 V

Table 2.1-2 LCD0 (LVDS) (CN16) pin assignment

LCD1 [CN17]

No	Signal Name	Description	SMARC Signal Path	Remarks
1	VCC	+3.3 V		
2	VCC	+3.3 V		
3	GND	GND		
4	GND	GND		
5	LVDS0-	LCD DATA	LVDS1_0-	
6	LVDS0+	LCD DATA	LVDS1_0+	
7	LVDS1-	LCD DATA	LVDS1_1-	
8	LVDS1+	LCD DATA	LVDS1_1+	
9	LVDS2-	LCD DATA	LVDS1_2-	
10	LVDS2+	LCD DATA	LVDS1_2+	
11	LVDS3-	LCD DATA	LVDS1_3-	
12	LVDS3+	LCD DATA	LVDS1_3+	
13	LVDS_CLK-	LCD DATA	LVDS1_CK-	
14	LVDS_CLK+	LCD DATA	LVDS1_CK+	
15	GND	GND		
16	UD/GPIO	UD Control/GPIO	GPIO7	3.3 V
17	BKLT_PWM	BackLight PWM	LCD1_BKLT_PWM	3.3 V
18	BKLT_EN	BackLight ENABLE	LCD1_BKLT_EN	3.3 V
19	I2C_CK	I2C CLOCK	I2C_LCD_CK	3.3 V
20	I2C_DAT	I2C DATA	I2C_LCD_DAT	3.3 V

Table 2.1-3 LCD1 (LVDS) (CN17) pin assignment

LVDS0 branches to LCD (TTL).

The LCD control signal is relayed through the LEVEL SHIFTER and bi-directionally converted to VDD_IO and 3.3 V.
The standard setting for VDD_IO voltage is 1.8 V. For details, see “1.9.1 VDD_IO Settings”.

2.2 LCD (TTL)

LCD(TTL) supports 1 channel of LVDS0.

It is converted to RGB parallel signals by the deserializer and can be connected to RGB parallel type LCD.

The connector is a 0.5 mm x 40 pin FFC connector (CN18) that can be directly connected to our “LCD-KIT-B02”, “LCD-KIT-C01”, “LCD-KIT-C02”, and “LCD-KIT-D02”.

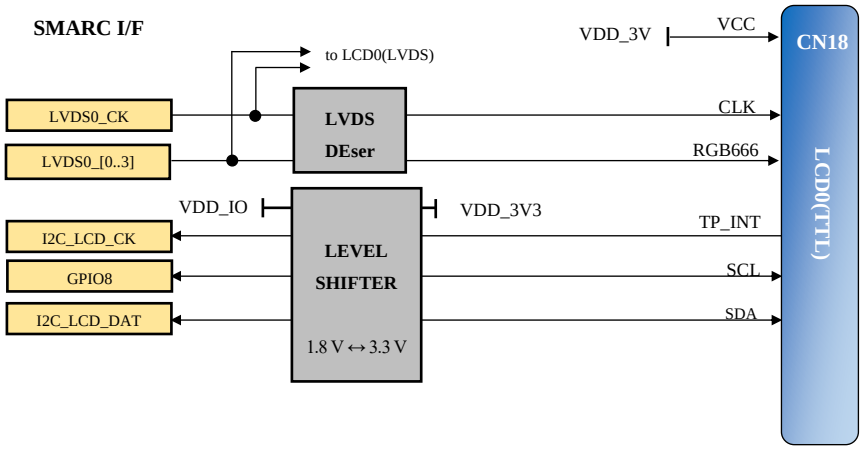


Fig 2.2-1 LCD (TTL) circuit connection configuration

The LCD control signal is relayed through the LEVEL SHIFTER and bi-directionally converted to VDD_IO and 3.3 V.

The standard setting for VDD_IO voltage is 1.8 V. For details, see “1.9.1 VDD_IO Settings”.

LCD0 TTL [CN18]

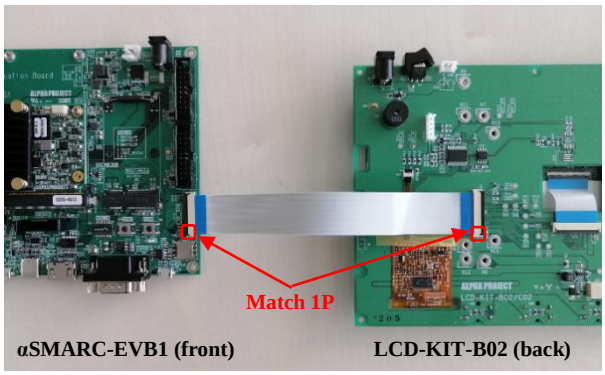
No	Signal Name	Description	SMARC Signal Path	Remarks
1	VDD_3V3	+3.3 V		
2	VDD_3V3	+3.3 V		
3	VDD_3V3	+3.3 V		
4	GND	GND		
5	GND	GND		
6	B0	LCD DATA Blue	LVDS0_DATA[0..2]	3.3 V
7	B1	LCD DATA Blue	LVDS0_DATA[0..2]	3.3 V
8	B2	LCD DATA Blue	LVDS0_DATA[0..2]	3.3 V
9	B3	LCD DATA Blue	LVDS0_DATA[0..2]	3.3 V
10	B4	LCD DATA Blue	LVDS0_DATA[0..2]	3.3 V
11	B5	LCD DATA Blue	LVDS0_DATA[0..2]	3.3 V
12	GND	GND		
13	G0	LCD DATA Green	LVDS0_DATA[0..2]	3.3 V
14	G1	LCD DATA Green	LVDS0_DATA[0..2]	3.3 V
15	G2	LCD DATA Green	LVDS0_DATA[0..2]	3.3 V
16	G3	LCD DATA Green	LVDS0_DATA[0..2]	3.3 V
17	G4	LCD DATA Green	LVDS0_DATA[0..2]	3.3 V
18	G5	LCD DATA Green	LVDS0_DATA[0..2]	3.3 V
19	R0	LCD DATA Red	LVDS0_DATA[0..2]	3.3 V
20	R1	LCD DATA Red	LVDS0_DATA[0..2]	3.3 V
21	R2	LCD DATA Red	LVDS0_DATA[0..2]	3.3 V
22	R3	LCD DATA Red	LVDS0_DATA[0..2]	3.3 V
23	R4	LCD DATA Red	LVDS0_DATA[0..2]	3.3 V

24	R5	LCD DATA Red	LVDS0_DATA[0..2]	3.3 V
25	GND	GND		
26	DE	Data Enable	LVDS0_DATA[0..2]	3.3 V
27	HSYNC	Horizontal Sync	LVDS0_DATA[0..2]	3.3 V
28	VSYNC	Vertical Sync	LVDS0_DATA[0..2]	3.3 V
29	GND	GND		
30	LCDCLK	LCD CLOCK	LVDS0_CK	3.3 V
31	GND	GND		
32	VDD_5V0	+5 V		
33	VDD_5V0	+5 V		
34	VDD_5V0	+5 V		
35	N.C	--		
36	SDA	I2C Data	I2C_LCD_DAT	3.3 V
37	SCL	I2C Clock	I2C_LCD_CK	3.3 V
38	TP_INT	Touch Panel Interrupt (Low Active)	GPIO8	3.3 V
39	N.C	--		
40	RESET	LCD RESET (Low Active)		3.3 V

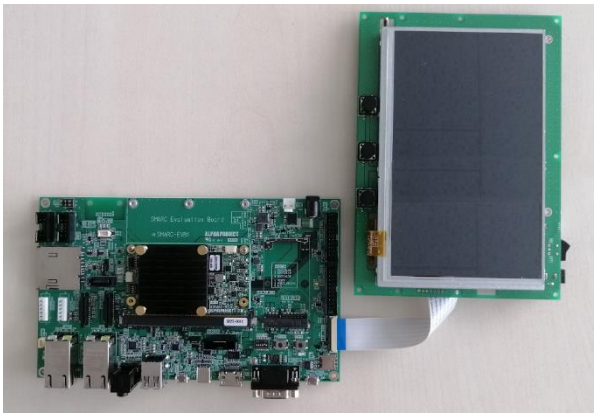
Table 2.2-2 LCD(TTL) (CN18) pin assignment

[Connecting the LCD-KIT]

Connect the LCD-KIT with the FFC cable supplied with the LCD-KIT. The following is a connection example with LCD-KIT-B02.



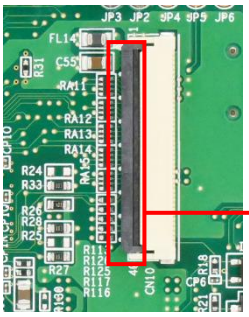
Connect 1P of CN18 and 1P of the LCD-KIT connector together. Either the front or the back of the FFC is fine.



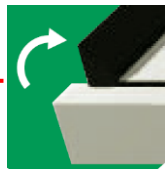
With the LCD-KIT laid flat, twist it 90˚ as shown in the photo to face the front. Be careful not to damage the FFC.

Handling FFC connectors

The precision structure of FFC connectors makes them prone to breakage. Handle them with care.



The lock is released by pushing the slider (lever) upward, so insert and remove the FFC. It is locked by pushing it down.



Release

Lock

2.3 Gigabit Ethernet

Gigabit Ethernet supports two channels, GBE0 and GB1.

It is connected to ETH0 (CN2) and ETH1 (CN3) of the RJ-45 connectors (built-in inductor).

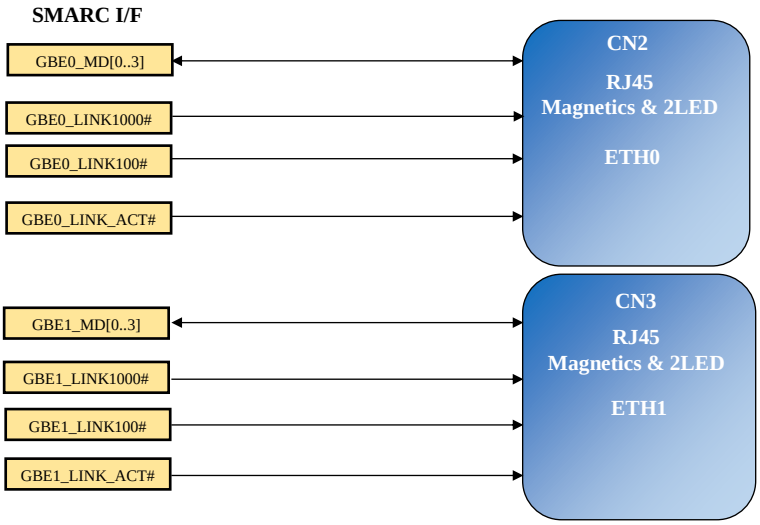


Fig 2.3-1 Gigabit Ethernet circuit connection configuration

2.4 CAMERA (MIPI-CSI2)

CAMERA supports two channels, CSI0 and CSI1.
It is connected to CH0 (CN13) and CH1 (CN14).

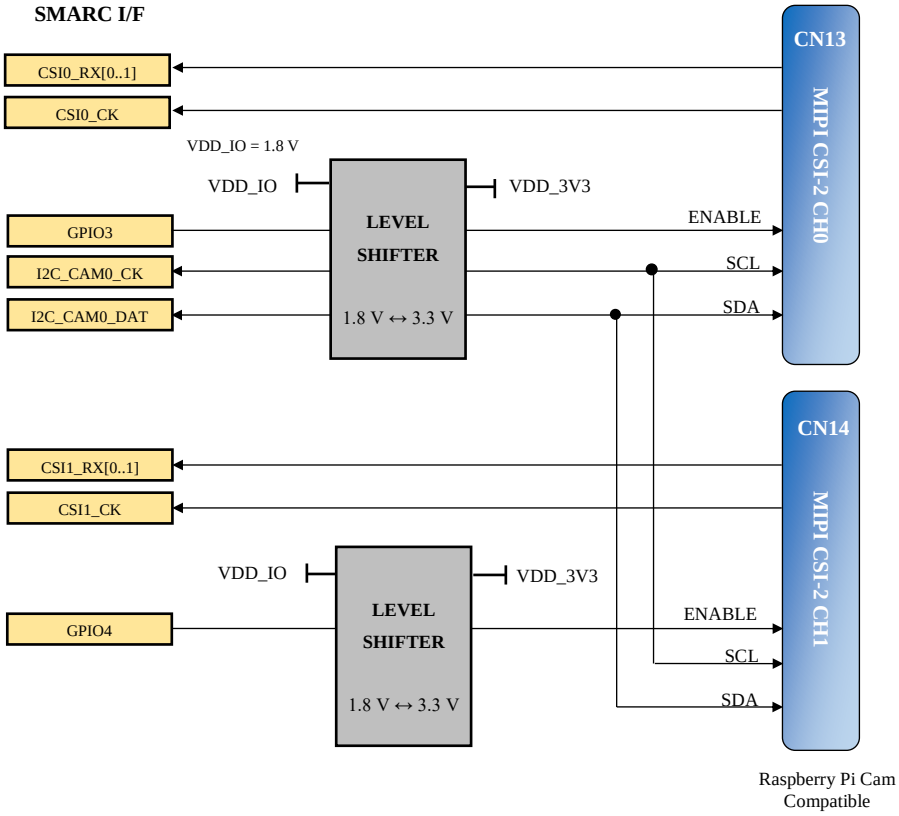


Fig 2.4-1 CAMERA circuit connection configuration

A “Raspberry Pi Camera Module V2” can be connected to the CH0 and CH1 connectors.

The CAMERA control signal is relayed through the LEVEL SHIFTER and bi-directionally converted to VDD_IO and 3.3 V.
The standard setting for VDD_IO voltage is 1.8 V. For details, see “1.9.1 VDD_IO Settings”.

CSI CH0 [CN13]

No	Signal Name	Description	SMARC Signal Path	Remarks
1	GND	GND		
2	CSI0_D0N	DATA IN	CSI0_RX0-	
3	CSI0_D0P	DATA IN	CSI0_RX0+	
4	GND	GND		
5	CSI0_D1N	DATA IN	CSI0_RX1-	
6	CSI0_D1P	DATA IN	CSI0_RX1+	
7	GND	GND		
8	CSI0_CLKN	CLOCK	CSI0_CK-	
9	CSI0_CLKP	CLOCK	CSI0_CK+	
10	GND	GND		
11	ENABLE	Camera Enable	GPIO3	3.3 V
12	N.C	--		
13	SCL	I2C CLOCK	I2C_CAM0_DAT	3.3 V
14	SDA	I2C DATA	I2C_CAM0_CK	3.3 V
15	VDD_3V3	+3.3 V		

Table 2.4-2 CAMERA CH0(CN13) pin assignment

CSI CH1 [CN14]

No	Signal Name	Description	SMARC Signal Path	Remarks
1	GND			
2	CSI0_D0N	DATA IN	CSI1_RX0-	
3	CSI0_D0P	DATA IN	CSI1_RX0+	
4	GND			
5	CSI0_D1N	DATA IN	CSI1_RX1-	
6	CSI0_D1P	DATA IN	CSI1_RX1+	
7	GND			
8	CSI0_CLKN	CLOCK	CSI1_CK-	
9	CSI0_CLKP	CLOCK	CSI1_CK+	
10	GND	GND		
11	ENABLE	Camera Enable	GPIO4	3.3 V
12	N.C	--		
13	SCL	I2C CLOCK	I2C_CAM1_DAT	3.3 V
14	SDA	I2C DATA	I2C_CAM1_CK	3.3 V
15	VDD_3V3	+3.3 V		

Table 2.4-3 CAMERA CH1(CN14) pin assignment

2.5 SD/SDIO

SD/SDIO supports 1 channel.

The SD card slot is for standard SD cards (SD1) and supports SD cards and SDIO cards.

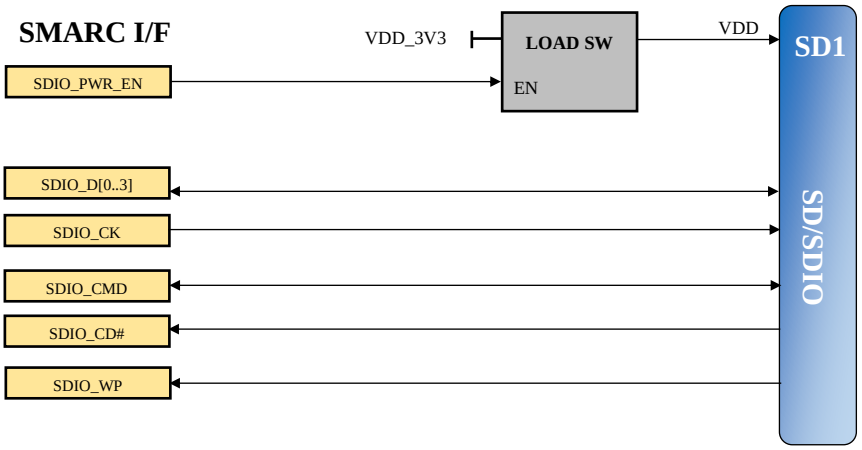


Fig 2.5-1 SD/SDIO circuit connection configuration

2.6 AUDIO I2S

AUDIO I2S supports 1 channel of I2S0.

It is equipped with an AUDIO stereo codec and supports 1 channel each for input and output.

It is connected to the 3.5 mm stereo headphone jack (CN15).

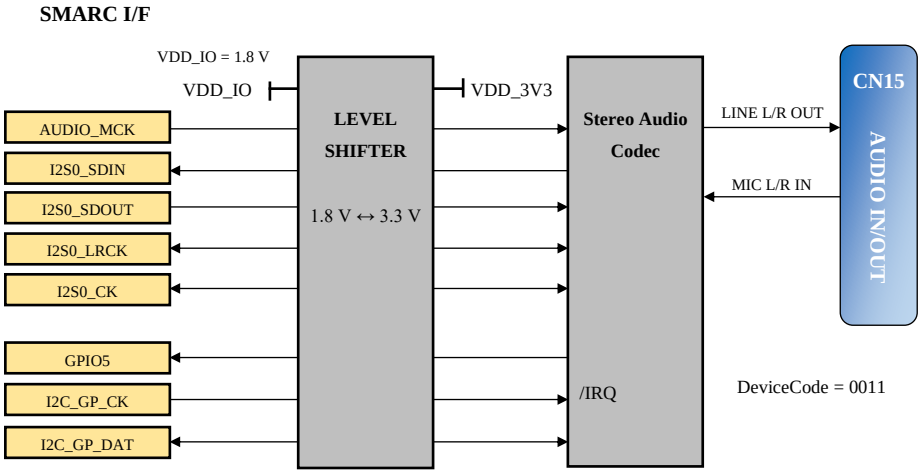


Fig 2.6-1 AUDIO I2S circuit connection configuration

The AUDIO I2S control signal is relayed through the LEVEL SHIFTER and bi-directionally converted to VDD_IO and 3.3 V.

The standard setting for VDD_IO voltage is 1.8 V. For details, see “1.9.1 VDD_IO Settings”.

Item	Min	Typ	Max	Unit	Remarks
Output Voltage Signal Level		0.56		V_{RMS}	VOLL, VOLR = 0x09
Output Gain	0		18	dB	dB
Output Power (R_L = 16Ω)		19		mW	mW
Output Power (R_L = 32Ω)	8	10		mW	mW

Table 2.6-2 Audio output interface: output characteristics

Item	Min	Typ	Max	Unit	Remarks
Microphone bias	1.5	1.525	1.55	V	I_{LOAD} = 1 mA
Output Voltage Signal Level		1.0		Vp-p	
Input Gain	0		30	dB	Programmable
Input impedance	30	50		KΩ	

Table 2.6-3 Audio microphone input interface: input characteristics

2.7 USB 2.0

USB 2.0 supports 2 channels, USB0 and USB1.
It is connected to USB Host/Function (CN10A/CN11) 1 channel, USB HOST (CN10B) 1 channel, and mimiPCIe 1 channel.
HOST is a Type-A connector and Function is a microB connector.

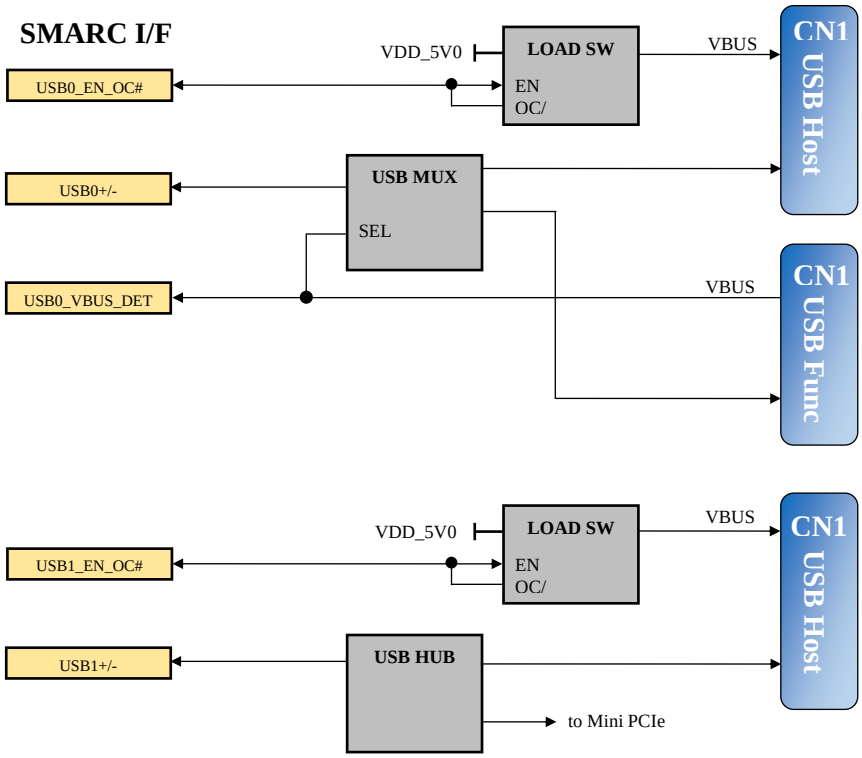


Fig 2.7-1 USB 2.0 circuit connection configuration

USB0 is exclusively used by Host (CN10A) and Function (CN11). If both Host and Function are connected, it will be switched to Function preferentially.
USB1 branches at the HUB and can be used simultaneously by Host (CN10B) and Host (mini PCIe).

2.8 USB3.0

USB 3.0 supports 1 channel of USB3.

It is connected to Type-C (CN9) and supports OTG (Dual-Role) function and can be used with Host and Function.

(Dual-Role Power and Power Delivery are not supported)

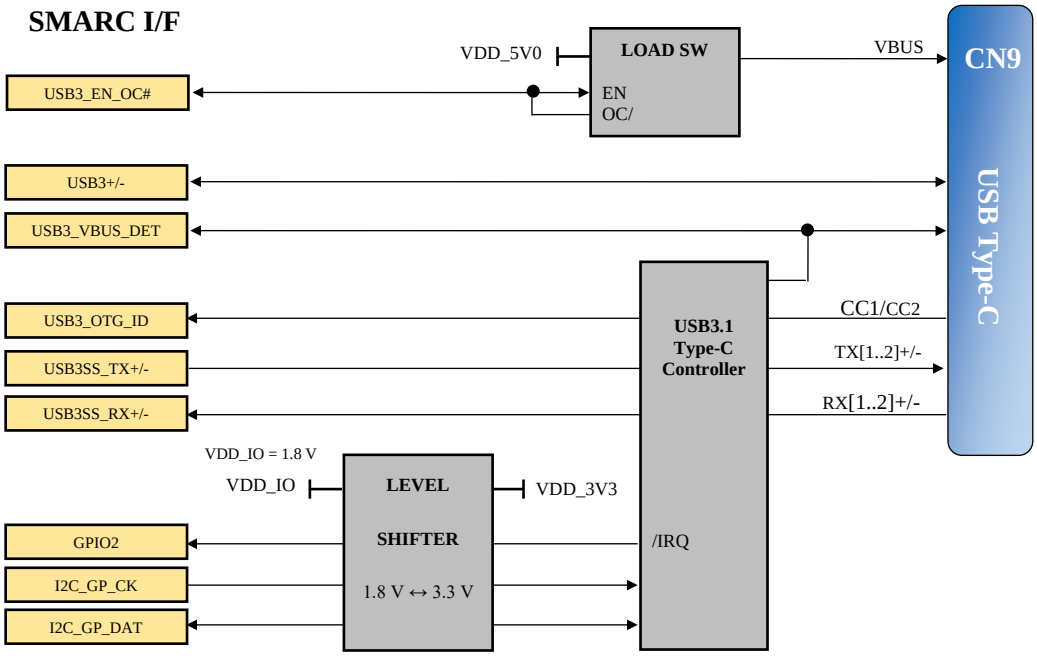


Fig 2.8-1 USB 3.0 circuit connection configuration

The I2C signal is relayed through the LEVEL SHIFTER and bi-directionally converted to VDD_IO and 3.3 V.

The standard setting for VDD_IO voltage is 1.8 V. For details, see “1.9.1 VDD_IO Settings”.

2.9 Serial Interface

The Serial Interface supports 4 channels, from SER0 to SER3.
COM0 (CN5) and COM1 (CN6) are assigned as RS232 and USB COM respectively.
COM2 (CN7) and COM3 (CON8) are 3.3 V TTL signals. By connecting the peripheral expansion adapter optional part, it can be converted to RS232, USB, RS485/RS422, Ethernet, etc.

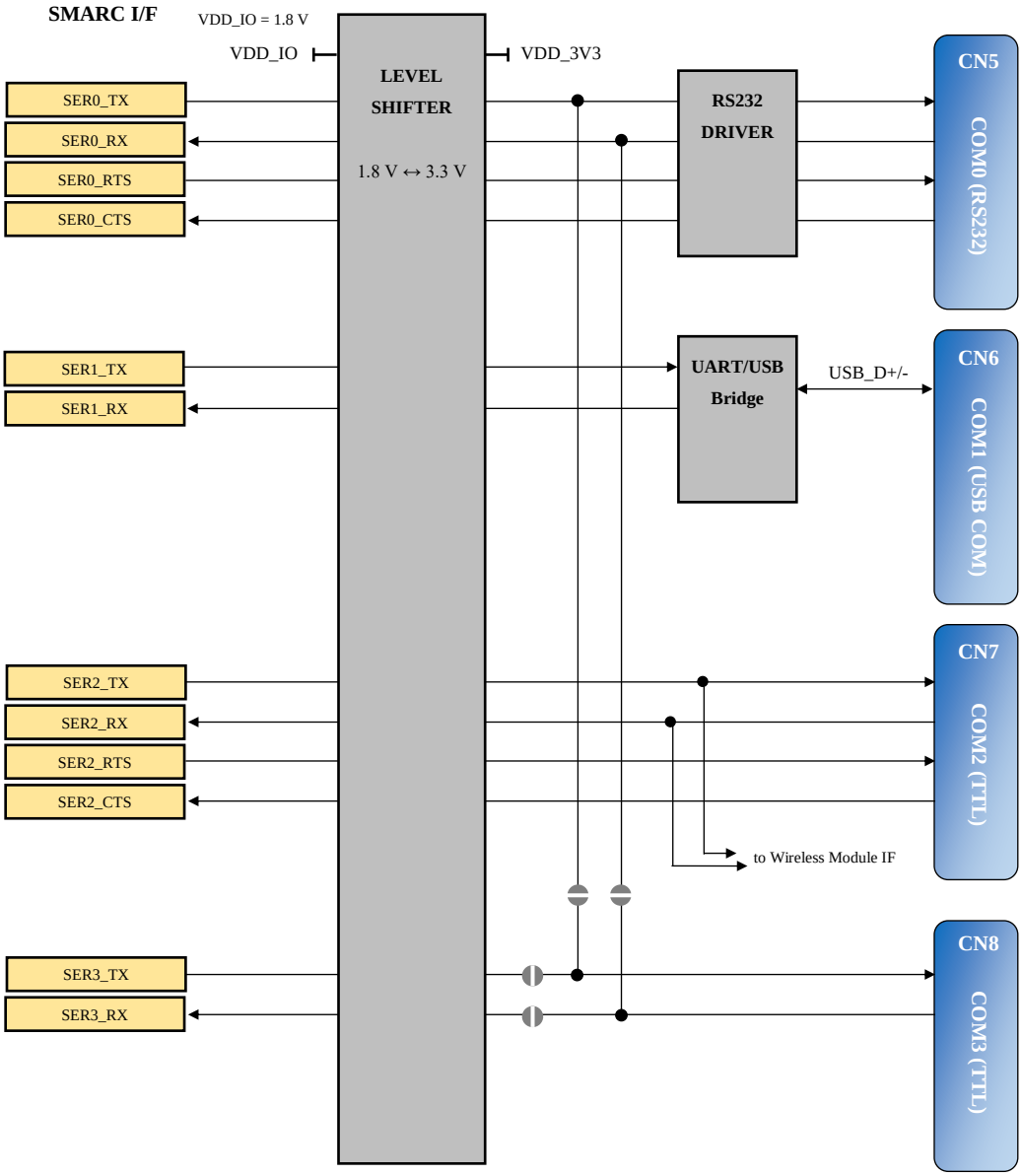


Fig 2.9-1 Serial Interface circuit connection configuration

The Serial Interface signal is relayed through the LEVEL SHIFTER and bi-directionally converted to VDD_IO and 3.3 V.
The standard setting for VDD_IO voltage is 1.8 V. For details, see “1.9.1 VDD_IO Settings”.

COM0 [CN5]

No	Signal Name	Description	SMARC Signal Path	Remarks
1	N.C	--		
2	RX	Receive data input	SER0_RX	RS232
3	TX	Transmit data output	SER0_TX	RS232
4	N.C	--		
5	GND	GND		
6	N.C	--		
7	RTS	RTS output	SER0_RTS	RS232
8	CTS	CTS input	SER0_CTS	RS232
9	N.C			

Table 2.9-2 COM0(CN5) pin assignment

COM2 [CN7]

No	Signal Name	Description	SMARC Signal Path	Remarks
1	RXD	Receive data input	SER2_RX	3.3 V
2	TXD	Transmit data output	SER2_TX	3.3 V
3	RTS	RTS output	SER2_RTS	3.3 V
4	CTS	CTS input	SER2_CTS	3.3 V
5	VCC	+3V3		
6	GND	GND		

Table 2.9-3 COM2(CN7) pin assignment

COM3 [CN8]

No	Signal Name	Description	SMARC Signal Path	Remarks
1	RXD	Receive data input	SER3_RX	3.3 V
2	TXD	Transmit data output	SER3_TX	3.3 V
3	RTS	Connect with 4 pin		3.3 V
4	CTS	Connect with 3 pin		3.3 V
5	VCC	+3V3		
6	GND			

Table 2.9-4 COM3 (CN8) pin assignment

2.10 CAN BUS

CAN supports two channels, CAN0 and CAN1 (CN4).
It is connected to a 2.5 mm x2 row box pin header (CN13).
It supports CAN FD with a maximum speed of 5 Mbps.

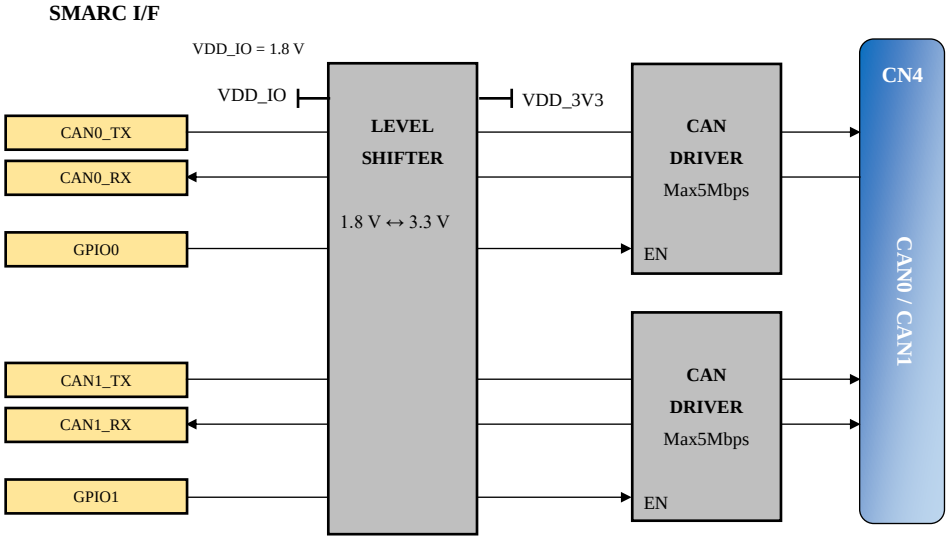


Fig 2.10-1 CAN BUS circuit connection configuration

The CAN and GPIO signals are relayed through the LEVEL SHIFTER and bi-directionally converted to VDD_IO and 3.3 V.
The standard setting for VDD_IO voltage is 1.8 V. For details, see “1.9.1 VDD_IO Settings”.

CAN [CN4]

No	Signal Name	Description	SMARC Signal Path	Remarks
1	VDD_5V0	+5 V		
2	CAN0H	CAN BUS +	CAN0_TX	
3	CAN0L	CAN BUS -	CAN0_RX	
4	GND	GND		
5	N.C	--		
6	VDD_5V0	+5 V		
7	CAN1H	CAN BUS +	CAN1_TX	
8	CAN1L	CAN BUS -	CAN1_RX	
9	GND	GND		
10	N.C	--		

Table 2.10-2 CAN BUS(CN4) pin assignment

2.11 PCI Express (mini PCIe)

PCI Express supports 1 channel of PCI_A.

It is connected to a mini PCIe slot, and can be used with wireless LAN, Bluetooth, cellular modules, etc.

It also supports USB and SIM cards.

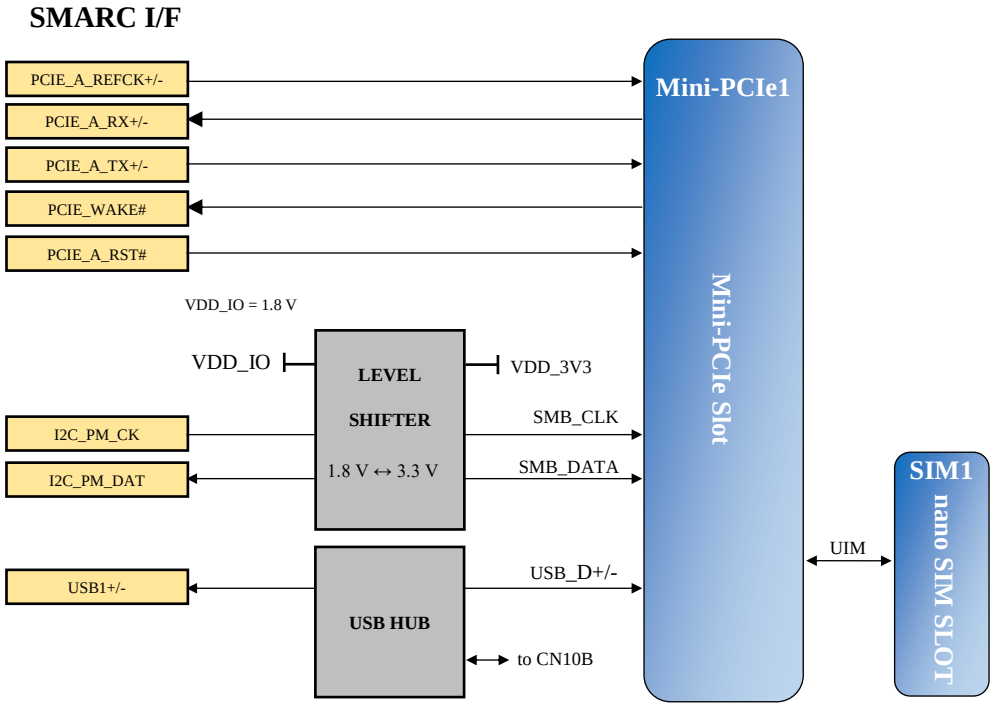


Fig 2.11-1 mini-PCIe circuit connection configuration

The I2C signal is relayed through the LEVEL SHIFTER and bi-directionally converted to VDD_IO and 3.3 V.

The standard setting for VDD_IO voltage is 1.8 V. For details, see “1.9.1 VDD_IO Settings”.

The mini PCIe slot supports full size. When using a half-size card, screw it with a spacer or use a conversion adapter.

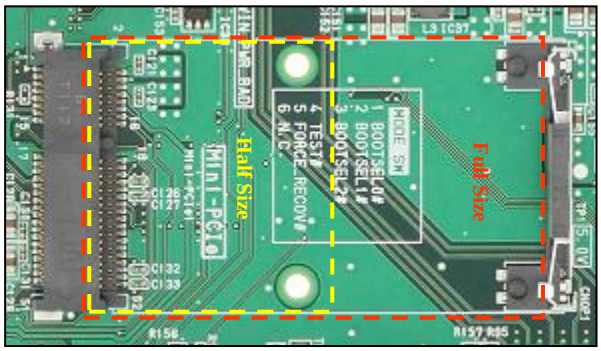


Fig 2.11-2 mini-PCIe Slot

Mini PCIe

No	Signal Name	SMARC Signal Path	No	Signal Name	SMARC Signal Path
1	WAKE#	PCIE_WAKE#	2	3.3V_AUX	
3	N.C		4	GND	
5	N.C		6	1.5 V	
7	CLKREQ#		8	UIM_PWR	
9	GND		10	UIM_DATA	
11	REFCLK-	PCIE_A_REFCK-	12	UIM_CLK	
13	REFCLK+	PCIE_A_REFCK+	14	UIM_RST	
15	GND		16	UIM_VPP	
17	N.C		18	GND	
19	N.C		20	N.C	
21	GND		22	PERST#	PCIE_A_RST#
23	PERN0	PCIE_A_RX-	24	3.3V_AUX	
25	PERP0	PCIE_A_RX+	26	GND	
27	GND		28	1.5 V	
29	GND		30	SMB_CLK	I2C_PM_CK
31	PETN0	PCIE_A_TX-	32	SMB_DATA	I2C_PM_DAT
33	PETP0	PCIE_A_TX+	34	GND	
35	GND		36	USB_D-	USB1-
37	GND		38	USB_D+	USB1+
39	3.3V_AUX		40	GND	
41	3.3V_AUX		42	N.C	
43	GND		44	N.C	
45	N.C		46	N.C	
47	N.C		48	1.5 V	
49	N.C		50	GND	
51	N.C		52	3.3V_AUX	

Table 2.11-3 mini PCIe Slot pin assignment

2.12 SATA

SATA supports 1 channel.

The connector is connected to a 7 pin standard SATA connector (CN21).

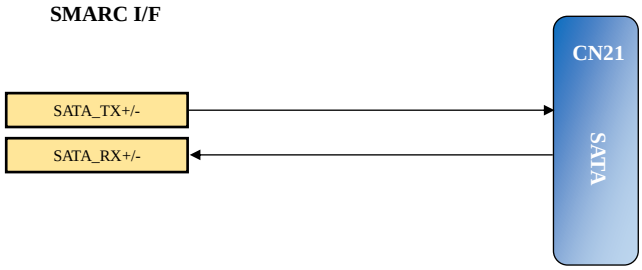


Fig 2.12-1 SATA circuit connection configuration

SATA [CN21]

No	Signal Name	Description	SMARC Signal Path	Remarks
1	GND	GND		
2	A+	Transmit Data +	SATA_TX+	
3	A-	Transmit Data +	SATA_TX-	
4	GND	GND		
5	B-	Receive Data+	SATA_RX-	
6	B+	Receive Data-	SATA_RX+	
7	GND	GND		

Table 2.12-2 SATA(CN21) pin assignment

2.13 HDMI

HDMI supports 1 channel.

The connector is connected to a standard HDMI connector (CN12).

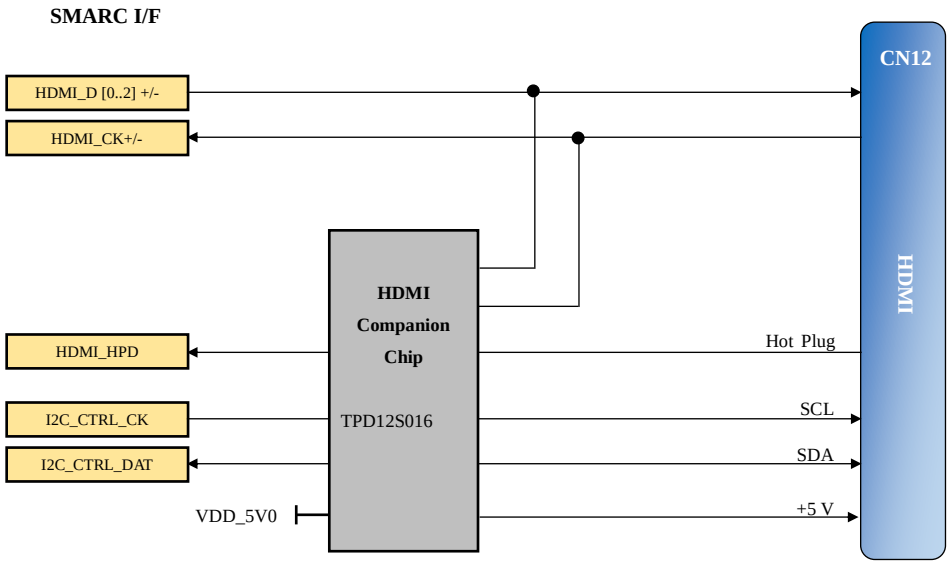


Fig 2.13-1 HDMI circuit connection configuration

HDMI [CN12]

No	Signal Name	SMARC Signal Path	No	Signal Name	SMARC Signal Path
1	Data2+	HDMI_D2+	2	Data2 Shield	
3	Data2-	HDMI_D2-	4	Data1+	HDMI_D1+
5	GND		6	Data1-	HDMI_D1-
7	Data0+	HDMI_D0+	8	Data0 Shield	
9	Data0-	HDMI_D0-	10	Clock+	HDMI_CK+
11	Clock Shield		12	Clock-	HDMI_CK-
13	CEC		14	N.C	
15	SCL	HDMI_CTRL_CK	16	SDA	HDMI_CTRL_DAT
17	DDC		18	+5 V	
19	HotPlg				

Table 2.13-2 HDMI(CN12) pin assignment

2.14 GPIO

GPIO supports 14 channels from GPIO0 to GPIO13.

GPIO is assigned to the GPIO connector (CN22) and control of each interface.

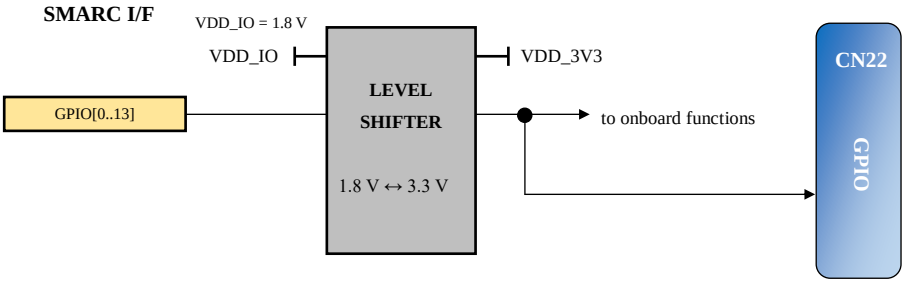


Fig 2.14-1 GPIO circuit connection configuration

GPIO	Function assignment	Input/Output	Other
GPIO0	CAN0 Silent Control	OUT	CN22
GPIO1	CAN1 Silent Control	OUT	CN22
GPIO2	USB3 Interrupt	IN(Int)	
GPIO3	CAMERA CSI0 Enable	OUT	CN22
GPIO4	CAMERA CSI1 Enable	OUT	CN22
GPIO5	AUDIO Codec Interrupt	IN(Int)	
GPIO6	LCD_LVDS0 UD/GPIO	OUT/IN	
GPIO7	LCD_LVDS1 UD/GPIO	OUT/IN	
GPIO8	LCD(TTL) TouchPanel Interrupt	IN(Int)	
GPIO9	Wireless Module Power enable	OUT	
GPIO10	Wireless Module Power Interrupt	IN(Int)	
GPIO11	Wireless Module Power Reset	OUT	CN22
GPIO12	Status LED1	OUT	CN22
GPIO13	Status LED2	OUT	CN22

Table 2.14-2 GPIO function assignment

The GPIO assigned to CN22 can be used for any application if the assigned function on the board is not used.

The GPIO signal is relayed through the LEVEL SHIFTER and bi-directionally converted to VDD_IO and 3.3 V.

The standard setting for VDD_IO voltage is 1.8 V. For details, see “1.9.1 VDD_IO Settings”.

GPIO [CN22]

No	Signal Name	SMARC Signal Path	No	Signal Name	SMARC Signal Path
1	VDD_3V3		2	GND	
3	GPIO0_3V3	GPIO0	4	GPIO1_3V3	GPIO1
5	GPIO3_3V3	GPIO3	6	GPIO4_3V3	GPIO4
7	GPIO11_3V3	GPIO11	8	GPIO12_3V3	GPIO12
9	GPIO13_3V3	GPIO13	10	N.C	

Table 2.14-3 GPIO(CN22) pin assignment

2.15 I2C

I2C supports 5 channels: I2C_CAM0, I2C_CAM1, I2C_PM, I2C_LCD, and I2C_GP.
Each channel is connected to the I2C connector (CN1) and each function.

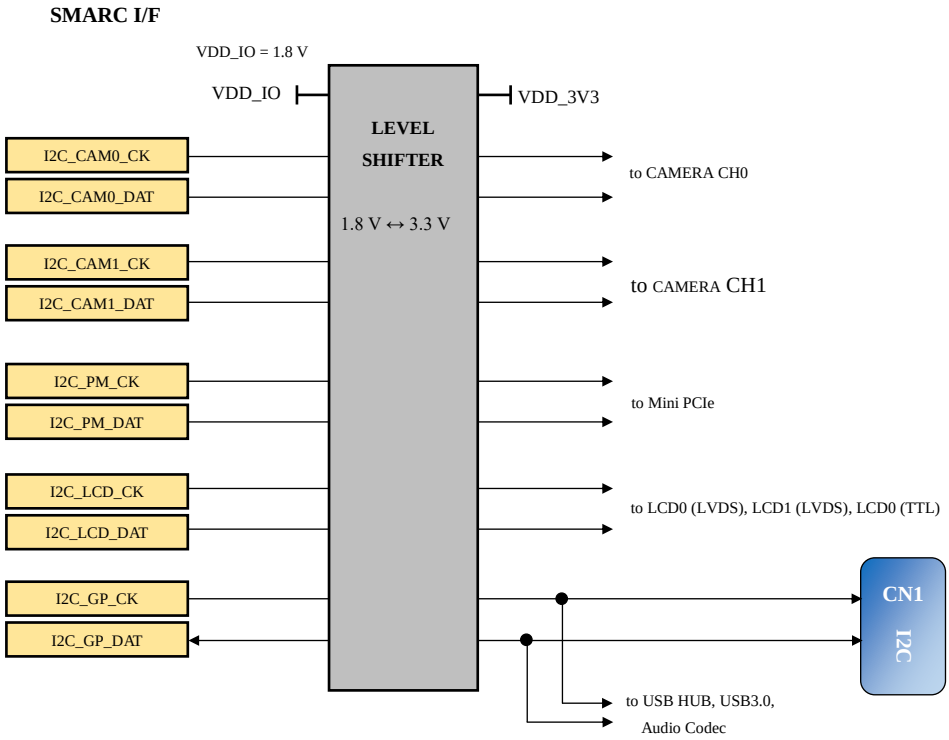


Fig 2.15-1 I2C circuit connection configuration

The I2C signal is relayed through the LEVEL SHIFTER and bi-directionally converted to VDD_IO and 3.3 V.
The standard setting for VDD_IO voltage is 1.8 V. For details, see “1.9.1 VDD_IO Settings”.

I2C [CN1]

No	Signal Name	Description	SMARC Signal Path	Remarks
1	SCL	I2C CLOCK	I2C_GP_CK	3.3 V
2	SDA	I2C DATA	I2C_GP_DAT	3.3 V
3	VDD_3V3	+3.3 V		
4	GND	GND		

Table 2.15-2 I2C(CN1) pin assignment

2.16 SPI

SPI supports 1 channel of SPI0.

SPI is connected to SPI connector (CN20) and Wireless Module Interface (CN19).

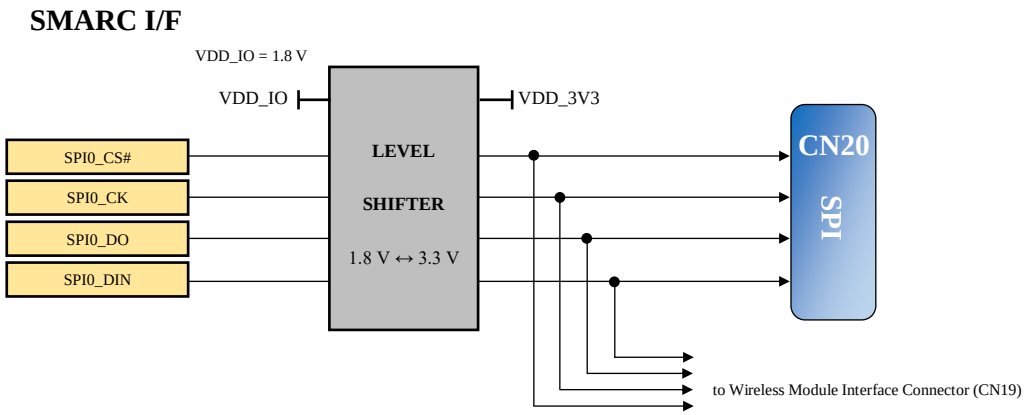


Fig 2.16-1 SPI circuit connection configuration

The SPI signal is relayed through the LEVEL SHIFTER and bi-directionally converted to VDD_IO and 3.3 V.

The standard setting for VDD_IO voltage is 1.8 V. For details, see “1.9.1 VDD_IO Settings”.

SPI [CN20]

No	Signal Name	Description	SMARC Signal Path	Remarks
1	VDD_3.3V	+3.3 V		
2	GND	GND		
3	SPI_MOSI	SPI MasterOut / SlaveIn	SPI0_DO	3.3 V
4	SPI_MISO	SPI MasterIn / SlaveOut	SPI0_DIN	3.3 V
5	SPI_CS	SPI Device Select Out	SPI0_CS#	3.3 V
6	SPI_CLK	SPI Clock Out	SPI_CK	3.3 V

Table 2.16-2 SPI (CN1) pin assignment

2.17 Mode SW

BOOT_SEL[0..2]#, TEST#, and FORCE_RECOV# are connected to Mode SW (SW1).

Open when OFF and Low (shorted to GND) when ON.

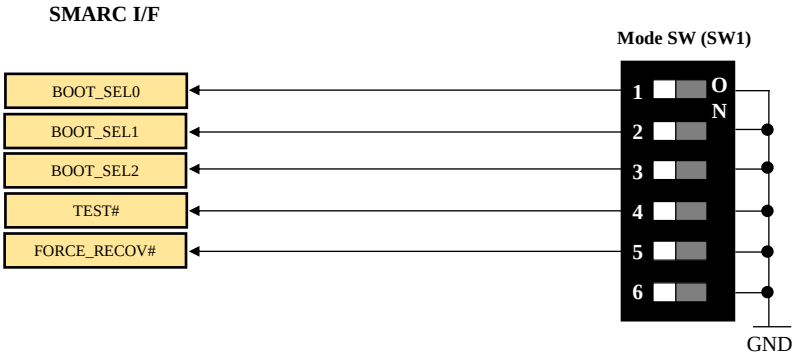


Fig 2.17-1 Mode SW circuit connection configuration

2.18 Wireless Module Interface

The Wireless Module Interface is compatible with the wireless LAN/Bluetooth module “WM-RP-10” and is controlled by SPI0 or SER2.
The connector is a 0.5 mm stacking connector.
WM-RP-10 is an optional part. Install it as necessary.

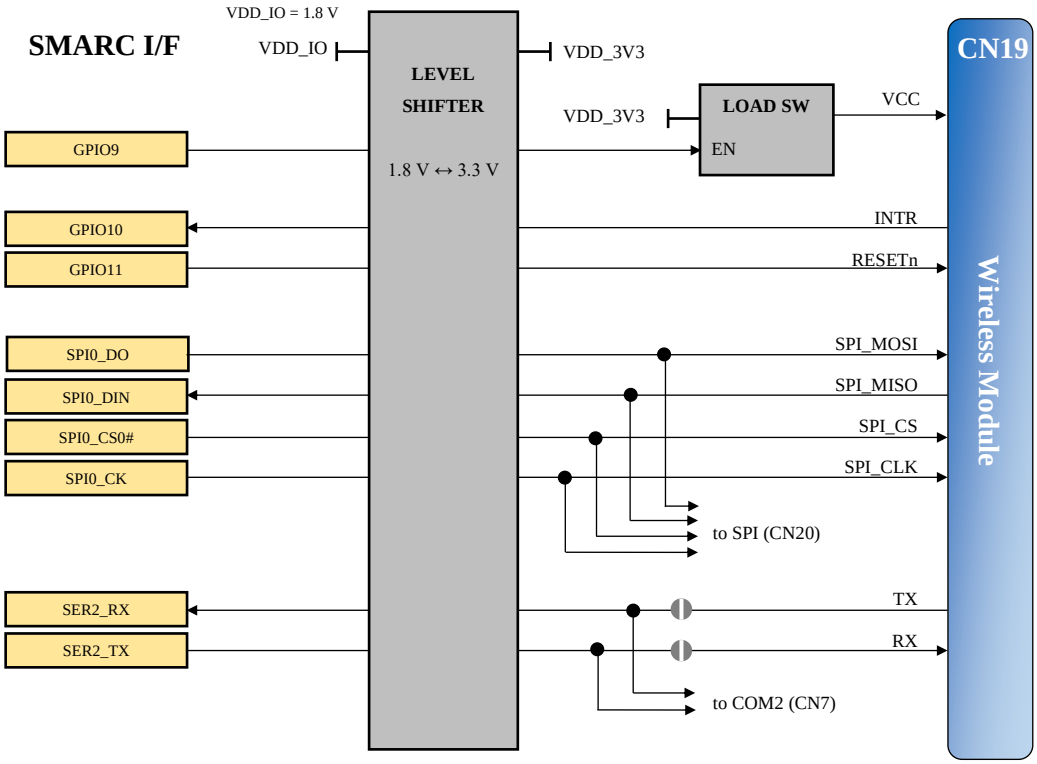


Fig 2.18-1 Wireless Module Interface circuit connection configuration

The SPI0, SER2, and GPIO signals are relayed through the LEVEL SHIFTER and bi-directionally converted to VDD_IO and 3.3 V.
The standard setting for VDD_IO voltage is 1.8 V. For details, see “1.9.1 VDD_IO Settings”.

2.19 Power Management

SMARC-EVB1 operates on a single 5 V power supply.

Each voltage is generated by the power circuit and output is controlled by the CARRIER_PWR_ON signal.

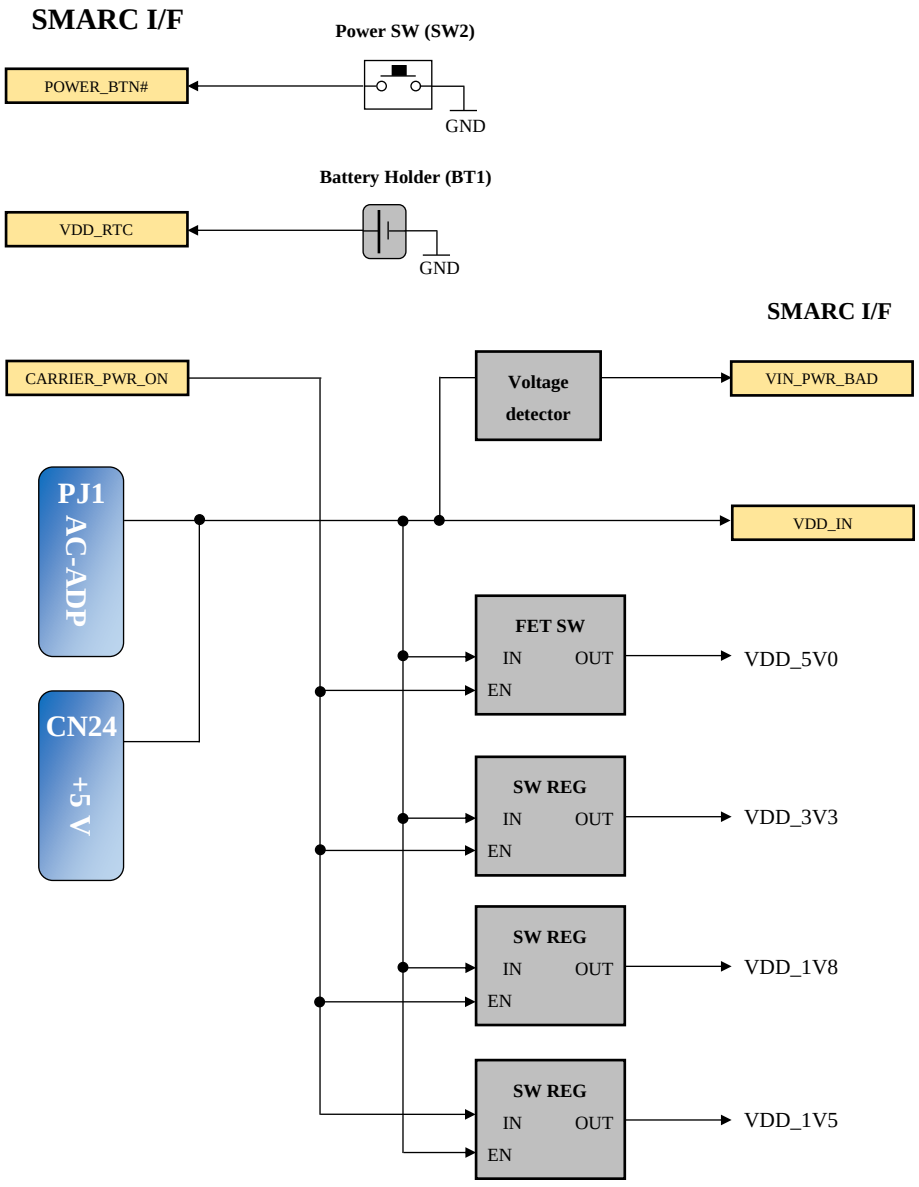


Fig 2.19-1 Power Management circuit connection configuration

2.20 Reset Control

The Reset Control circuit activates the carrier board's internal RESET signal (puts it in the RESET state) when VDD_3V3 is less than 3.0 V or when RESET_OUT#, WDT_TIME_OUT#, or CARRIER_STBY# become active.

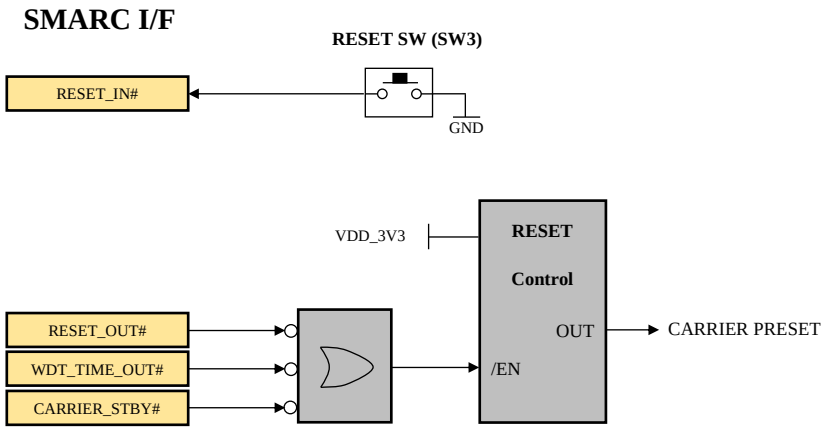


Fig 2.20-1 Reset Control circuit connection configuration

Handling of RESET_OUT#, WDT_TIME_OUT#, and CARRIER_STBY# on the carrier board is optional.
Design appropriately according to the application.

3. Technical Data

3.1 External Dimensions

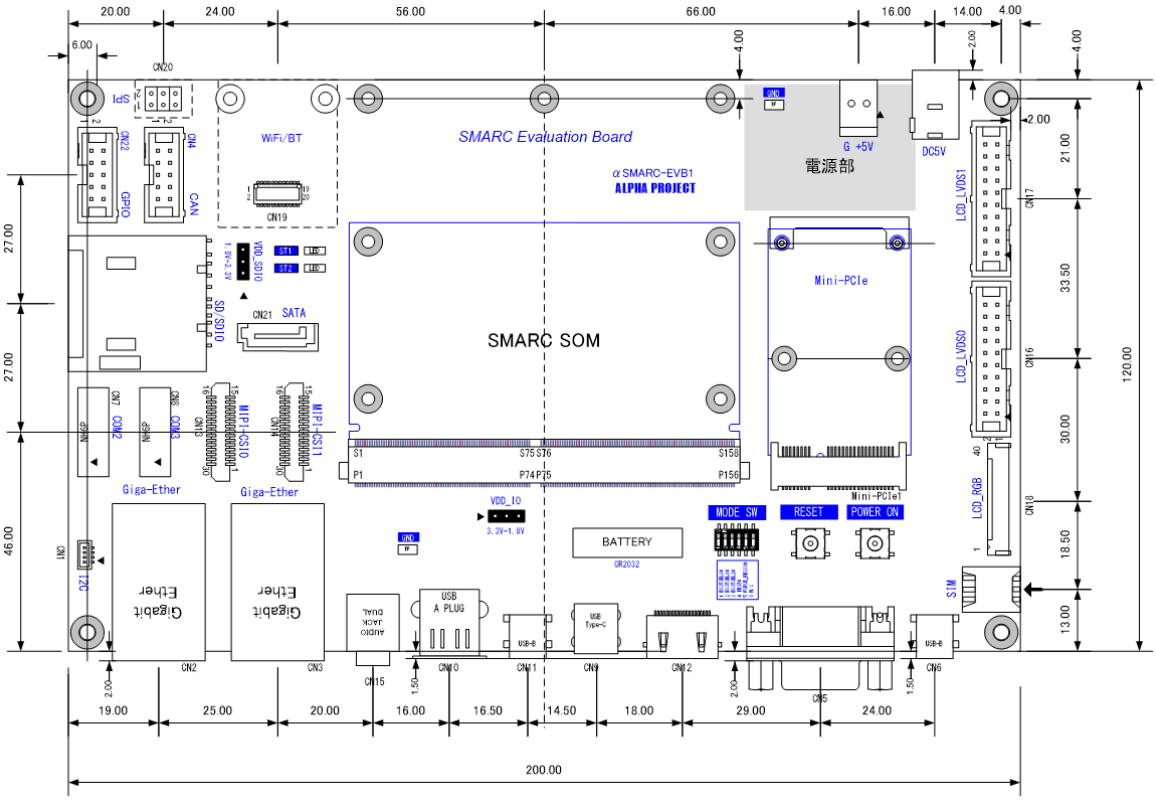


Fig 3.1-1 αSMARC-EVB1 dimensional drawing

3.2 Circuit Diagram

Circuit diagrams are only available to product users. Download them from the product page of our website.

4. Related Products

4.1 SMARC 2.1 SoM

The SoM (System On Module) conforms to the SMARC standard. It can be evaluated by installing it in “αSMARC_EVB1”.

αSMARC-RZ/G2E

αSMARC-IMX8MM

αSMARC-IMX8MN

4.2 αSMARC Development Kit

“αSMARC development kit” is a development kit that includes a αSMARC series SoM (System On Module), carrier board, AC adapter, and Linux BSP.

It includes all the equipment and software necessary for development, so development can start right away.

αSMARC series SoM

αSMARC-EVB1

AC adapter

Development Kit Name	Kit Contents
αSMARC-RZ/G2E-KIT	αSMARC-RZ/G2E, αSMARC-EVB1, LinuxBSP, AC adapter
αSMARC-IMX8MM-KIT	αSMARC-IMX8MM , αSMARC-EVB1, LinuxBSP, AC adapter, Heat sink
αSMARC-IMX8MN-KIT	αSMARC-IMX8MN , αSMARC-EVB1, LinuxBSP, AC adapter, Heat sink

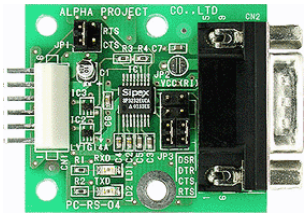
4.3 Card-Edge Connector

Alpha Project can provide MXM3.0 card-edge connectors that are compatible with SMARC modules.

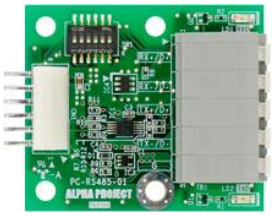
Please inquire with us.

4.4 Peripheral Expansion Adapter

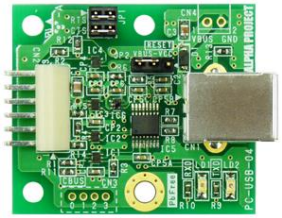
Interface functions can be added by connecting a peripheral expansion adapter to the UART connector (CN7, CN8).



PC-RS-04



PC-RS485-01A



PC-USB-04

Product Name	Function	Function Details
PC-RS-04	RS232C converter	This adapter converts the serial interface to RS232 level.
PC-RS485-01A	RS422/485 converter	This adapter converts the serial interface to RS422 or RS485 level.
PC-USB-04	USB converter	This adapter converts a serial interface to a USB function (virtual COM port).

*Information as of July 2023, subject to change without notice.

4.5 Touch Panel LCD Kit

You can easily evaluate the touch panel system by connecting the LCD kit to the LCD (TTL) connector (CN18).

Product Name	Product Function	Remarks
LCD-KIT-C02	7 inch WVGA LCD kit with resistive touch panel	Single Touch
LCD-KIT-D02	4.3 inch WQVGA LCD kit with capacitive touch panel	Multi-touch compatible (5 points)

Check the compatibility status of the Linux driver in advance.

5. Product Support Information

Alpha Project's product support accepts user registration, repairs, inquiries, etc. See the page below for information.

Product Support Page*

https://www.apnet.co.jp/support/index.html

* Japanese site only.

User Registration

Please do user registration before requesting repairs or making inquiries.
Registered users also get notices of version upgrades and the latest information by email.

Warranty & Repair Applications

Alpha Project provides initial defect replacement and free warranty in accordance with the product warranty regulations.
We offer paid repairs for products that have passed the warranty period.
You can apply from the product warranty and product repair options on the product support page.

Inquiries

We accept general questions about our products.
When you inquire, make sure to include the product name, use environment, use method, and problems in the details.

Please note that we do not accept inquiries about the following content.

- ■ Questions about the circuit operation of this product and method of using CPUs and peripheral devices
- ■ Questions about the design methods and operations of user circuits
- ■ Guidance on operation of related tools
- ■ Other questions outside the scope of product specifications and problems that should be solved by customers' technology

Please note that Alpha Project does not accept questions about customers' individual software.
Customers who wish to receive support will be served individually for a fee. See "6. Information on Engineering Services".

6. Information on Engineering Services

Alpha Project accepts orders for custom products and system development based on our products.
We provide integrated service from design to OEM supply according to customers specifications.
For details, contact our sales office.

Information on Engineering Services*

https://www.apnet.co.jp/engineering/index.html

Inquiries

sales@apnet.co.jp

* Japanese site only.

Revision History

Version Number	Date	Revision Contents
Version 1.0	July 26, 2023	Create a new entry
Version 2.0	October 2, 2023	Update address.

About this document

■ The contents of this document are subject to change without notice.
■ The content of this document has been prepared with the utmost care. However, if you find any suspicious parts or mistakes, please contact us.
■ Please note that Alpha Project Co., Ltd. does not take responsibility for any damages that may occur as a result of operating the application based on the contents of this document.
■ The original file of this document is Japanese. If there is any inconsistency in description, the original one has priority of explanation.

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